Reconfigurable I/O

NI 783*x*R User Manual

Reconfigurable I/O Devices for
PCI/PXI/CompactPCI Bus Computers

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Consult the FCC Web site at `www.fcc.gov` for more information.

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Federal Communications Commission

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Canadian Department of Communications

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* The CE marking Declaration of Conformity contains important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments 783*x*R devices and contains information about programming and using the devices.

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

— This icon denotes a note, which alerts you to important information.

— This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the device, refer to the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

italic — Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

NI 783*x*R — NI 783*x*R refers to all PXI and PCI R Series devices with analog and digital I/O.

Reconfigurable I/O Documentation

The *NI 783xR User Manual* is one piece of the documentation set for your reconfigurable I/O system and application. Depending on the hardware and software you use for your application, you could have any of several types of documentation. The documentation includes the following documents:

- *Getting Started with the NI 783xR*—This document lists what you need to get started, describes how to unpack and install the hardware and software, and contains information about connecting I/O signals to the NI 783*x*R.
- *LabVIEW FPGA Module Release Notes*—This document contains information about installing and getting started with the LabVIEW FPGA Module. Select **Start»Program Files»National Instruments»<LabVIEW>»Module Documents»LabVIEW FPGA»Release Notes** to view this document.
- *LabVIEW FPGA Module User Manual*—This manual describes how to use the LabVIEW FPGA Module to create virtual instruments (VIs) that run on the NI 783*x*R. Select **Start»Program Files»National Instruments»<LabVIEW>»Module Documents»FPGA User Interface** to view this document.
- *FPGA Interface User Guide*—This manual describes how to control and communicate with FPGA VIs running on R Series devices. Select **Start»Program Files»National Instruments»<LabVIEW>» Module Documents»LabVIEW FPGA»LabVIEW FPGA Module User Manual** to view this document.
- *LabVIEW Help*—This help file contains information about using LabVIEW, the LabVIEW FPGA Module, and the LabVIEW Real-Time Module with the NI 783*x*R. Select **Help»VI, Function, & How-To Help** in LabVIEW to view the *LabVIEW Help*.
- *LabVIEW Real-Time Module User Manual*—This manual contains information about how to build deterministic applications using the LabVIEW Real-Time Module.

Related Documentation

The following documents contain information you might find helpful:

- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone`
- *PICMG CompactPCI 2.0 R3.0*
- *PXI Hardware Specification Revision 2.1*
- *PXI Software Specification Revision 2.1*

1 Introduction

This chapter describes the NI 783*x*R, the concept of the Reconfigurable I/O (RIO) device, optional software and equipment for using the NI 783*x*R, and safety information about the NI 783*x*R.

About the NI 783*x*R

The NI 783*x*R devices are R Series RIO devices with 16-bit analog input (AI) channels, 16-bit analog output (AO) channels, and digital I/O (DIO) lines.

- The NI PXI-7830R and NI PCI-7830R have four independent AI channels, four independent AO channels, and 56 DIO lines.
- The NI PXI-7831R/7833R and NI PCI-7831R/7833R have eight independent AI channels, eight independent AO channels, and 96 DIO lines.

A user-reconfigurable FPGA (Field-Programmable Gate Array) controls the digital and analog I/O lines on the NI 783*x*R. The FPGA on the R Series device allows you to define the functionality and timing of the device. You can change the functionality of the FPGA on the R Series device in LabVIEW using the LabVIEW FPGA Module to create and download a custom virtual instrument (VI) to the FPGA. Using the FPGA Module, you can graphically design the timing and functionality of the R Series device. If you only have LabVIEW but not the FPGA Module, you cannot create new FPGA VIs, but you can create VIs that run on Windows or a LabVIEW Real-Time (RT) target to control existing FPGA VIs.

Some applications require tasks such as real-time, floating-point processing or datalogging while performing I/O and logic on the R Series device. You can use the LabVIEW Real-Time Module to perform these additional applications while communicating with and controlling the R Series device.

The R Series device contains Flash memory to store a startup VI for automatic loading of the FPGA when the system is powered on.

The NI 783*x*R uses the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. The NI PCI-783*x*R accesses the RTSI bus through a RTSI cable connected between devices. The NI PXI-783*x*R accesses the RTSI bus through the PXI trigger lines implemented on the PXI backplane.

Refer to Appendix A, *Specifications*, for detailed NI 783*x*R specifications.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1*. If you use a PXI-compatible plug-in card in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you still can use the basic plug-in card functions. For example, the RTSI bus on the R Series device is available in a PXI chassis but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The R Series device works in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R3.0* core specification.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. Table 1-1 lists the J2 pins used by the NI 783*x*R. The NI 783*x*R is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the R Series device is still compatible as long as those pins on the sub-bus are disabled by default and are never enabled.

Caution Damage can result if the J2 lines are driven by the sub-bus.

Table 1-1. Pins Used by the NI PXI-783*x*R

NI PXI-783*x*R Signal	PXI Pin Name	PXI J2 Pin Number
PXI Trigger<0..7>	PXI Trigger<0..7>	A16, A17, A18, B16, B18, C18, E16, E18
PXI Clock 10 MHz	PXI Clock 10 MHz	E17
PXI Star Trigger	PXI Star Trigger	D17
LBLSTAR<0..12>	LBL<0..12>	A1, A19, C1, C19, C20, D1, D2, D15, D19, E1, E2, E19, E20
LBR<0..12>	LBR<0..12>	A2, A3, A20, A21, B2, B20, C3, C21, D3, D21, E3, E15, E21

Overview of Reconfigurable I/O

This section explains reconfigurable I/O and describes how to use the LabVIEW FPGA Module to build high-level functions in hardware.

Refer to Chapter 2, *Hardware Overview of the NI 783xR*, for descriptions of the I/O resources on the NI 783*x*R.

Reconfigurable I/O Concept

The NI 783*x*R is based on a reconfigurable FPGA core surrounded by fixed I/O resources for analog and digital input and output. You can configure the behavior of the reconfigurable FPGA to match the requirements of the measurement and control system. You can implement this user-defined behavior as an FPGA VI to create an application-specific I/O device.

Flexible Functionality

Flexible functionality allows the NI 783*x*R to match individual application requirements and to mimic the functionality of fixed I/O devices. For example, you can configure an R Series device in one application for three 32-bit quadrature encoders and then reconfigure the R Series device in another application for eight 16-bit event counters.

You also can use the R Series device with the LabVIEW Real-Time Module in timing and triggering applications, such as control and hardware-in-the-loop (HIL) simulations. For example, you can configure the R Series device for a single timed loop in one application and then reconfigure the device in another application for four independent timed loops with separate I/O resources.

User-Defined I/O Resources

You can create your own custom measurements using the fixed I/O resources. For example, one application might require an event counter that increments when a rising edge appears on any of three digital input lines. Another application might require a digital line to be asserted after an analog input exceeds a programmable threshold.

Device-Embedded Logic and Processing

You can implement LabVIEW logic and processing in the FPGA of the R Series device. Typical logic functions include Boolean operations, comparisons, and basic mathematical operations. You can implement multiple functions efficiently in the same design, operating sequentially or in parallel. You also can implement more complex algorithms such as control loops. You are limited only by the size of the FPGA.

Reconfigurable I/O Architecture

Figure 1-1 shows an FPGA connected to fixed I/O resources and a bus interface. The fixed I/O resources include A/D converters (ADCs), D/A converters (DACs), and digital I/O lines.

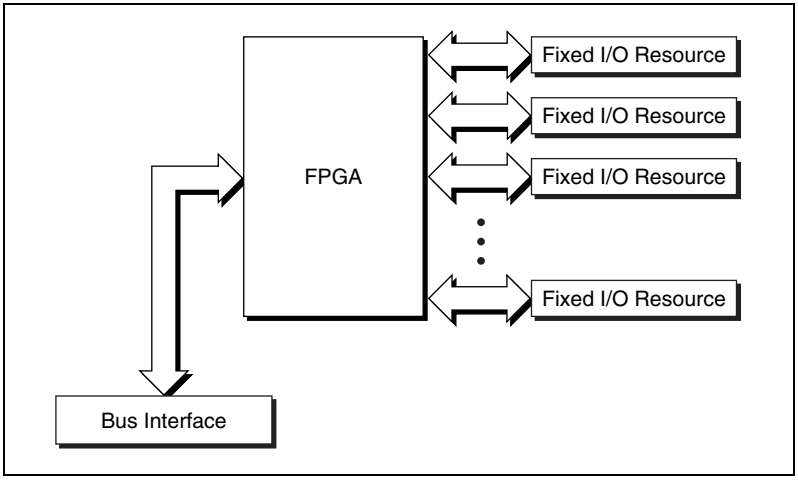


Figure 1-1. High-Level FPGA Functional Overview

Software accesses the R Series device through the bus interface, and the FPGA connects the bus interface and the fixed I/O to make possible timing, triggering, processing, and custom I/O measurements using the LabVIEW FPGA Module.

The FPGA logic provides timing, triggering, processing, and custom I/O measurements. Each fixed I/O resource used by the application uses a small portion of the FPGA logic that controls the fixed I/O resource. The bus interface also uses a small portion of the FPGA logic to provide software access to the device.

The remaining FPGA logic is available for higher-level functions such as timing, triggering, and counting. The functions use varied amounts of logic.

You can place useful applications in the FPGA. How much FPGA space your application requires depends on your need for I/O recovery, I/O, and logic algorithms.

The FPGA does not retain the VI when the R Series device is powered off, so you must reload the VI each time you power on the device. You can load the VI from onboard Flash memory or from software over the bus interface. One advantage to using Flash memory is that the VI can start executing almost immediately after power up, instead of waiting for the computer to completely boot and load the FPGA. Refer to the *LabVIEW FPGA Module User Manual* for more information about how to store your VI in Flash memory.

Reconfigurable I/O Applications

You can use the LabVIEW FPGA Module to create or acquire new VIs for your application. The FPGA Module allows you to define custom functionality for the R Series device using a subset of LabVIEW functionality. Refer to the FPGA Module examples located in the `<LabVIEW>\examples\FPGA` directory for examples of FPGA VIs.

Software Development

You can use LabVIEW with the LabVIEW FPGA Module to program the NI 783*x*R. To develop real-time applications that control the NI 783*x*R, use LabVIEW with the LabVIEW Real-Time Module.

LabVIEW FPGA Module

The LabVIEW FPGA Module enables you to use LabVIEW to create VIs that run on the FPGA of the R Series device. Use the FPGA Module VIs and functions to control the I/O, timing, and logic of the R Series device and to generate interrupts for synchronization. Refer to the *LabVIEW FPGA Interface User Guide*, available by selecting **Start»Program Files»National Instruments»<LabVIEW>»Module Documents»**

FPGA Interface User Guide, for information about the FPGA Interface functions.

You can use Interactive Front Panel Communication to communicate directly with the VI running on the FPGA. You can use Programmatic FPGA Interface Communication to programmatically control and communicate with FPGA VIs from host VIs.

Use the FPGA Interface functions when you target LabVIEW for Windows or an RT target to create host VIs that wait for interrupts and control the FPGA by reading and writing the FPGA VI running on the R Series device.

Note If you use the R Series device without the FPGA Module, you can use the Download VI or Attributes to Flash Memory utility available by selecting **Start»Program Files» National Instruments»NI-RIO** to download precomplied FPGA VIs to the Flash memory of the R Series device. This utility is installed by the NI-RIO CD. You also can use the utility to configure the analog input mode, to synchronize the clock on the R Series device to the PXI clock (for NI PXI-783*x*R only), and to configure when the VI loads from Flash memory.

LabVIEW Real-Time Module

The LabVIEW Real-Time Module extends the LabVIEW development environment to deliver deterministic, real-time performance.

You can write host VIs that run in Windows or on RT targets to communicate with FPGA VIs that run on the NI 783*x*R. You can develop real-time VIs with LabVIEW and the LabVIEW Real-Time Module, and then download the VIs to run on a hardware target with a real-time operating system. The LabVIEW Real-Time Module allows you to use the NI 783*x*R in RT Series PXI systems being controlled in real time by a VI.

The NI 783*x*R is designed as a single-point AI, AO, and DIO complement to the LabVIEW Real-Time Module. Refer to the *LabVIEW Real-Time Module User Manual* and the *LabVIEW Help*, available by selecting **Help»VI, Function, & How-To Help**, for more information about the LabVIEW Real-Time Module.

Cables and Optional Equipment

National Instruments offers a variety of products you can use with R Series devices, including cables, connector blocks, and other accessories, as shown in Table 1-2.

Table 1-2. Cables and Accessories

Cable	Cable Description	NI 783*x*R Connector	Accessories
SH68-C68-S	Shielded 68-pin VHDCI male connector to female 0.050 series D-type connector. The cable is constructed with 34 twisted wire pairs and an overall shield.	MIO or DIO	Connects to the following standard 68-pin screw terminal blocks: • SCB-68 • CB-68LP • CB-68LPR • TBX-68
SHC68-68-RMIO	Shielded 68-pin VHDCI male connector to female 0.050 series D-type connector. The cable is constructed with individually shielded twisted-pairs for the analog input channels plus an additional shield around all the analog signals. This cable provides superior noise immunity on the MIO connector.	MIO only	Connects to the following standard 68-pin screw terminal blocks: • SCB-68 • CB-68LP • CB-68LPR • TBX-68

Table 1-2. Cables and Accessories (Continued)

Cable	Cable Description	NI 783*x*R Connector	Accessories
NSC68-262650	Non-shielded cable connects from 68-pin VHDCI male connector to two 26-pin female headers plus one 50-pin female header. The pinout of these headers allows for direct connection to 5B backplanes for analog signal conditioning and SSR backplanes for digital signal conditioning.	MIO only	26-pin headers can connect to the following 5B backplanes for analog signal conditioning: • 5B08 (8-channel) • 5B01 (16-channel) 50-pin header can connect to the following SSR backplanes for digital signal conditioning: • 8-channel backplane • 16-channel backplane • 32-channel backplane
NSC68-5050	Non-shielded cable connects from 68-pin VHDCI male connector to two 50-pin female headers. The pinout of these headers allows for direct connection to SSR backplanes for digital signal conditioning.	DIO only	50-pin headers can connect to the following SSR backplanes for digital signal conditioning: • 8-channel backplane • 16-channel backplane • 32-channel backplane

Refer to Appendix B, *Connecting I/O Signals*, for more information about using these cables and accessories to connect I/O signals to the NI 783*x*R. Refer to `ni.com/products` or contact the sales office nearest to you for the most current cabling options.

Custom Cabling

NI offers a variety of cables for connecting signals to the NI 783*x*R. If you need to develop a custom cable, a nonterminated shielded cable is available from NI. The SHC68-NT-S connects to the NI 783*x*R VHDCI connectors on one end of the cable. The other end of the cable is not terminated. This cable ships with a wire list identifying the wires that correspond to each NI 783*x*R pin. Using this cable, you can quickly connect the NI 783*x*R

signals that you need to the connector of your choice. Refer to Appendix B, *Connecting I/O Signals*, for the NI 783*x*R connector pinouts.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the NI 783*x*R.

Do *not* operate the NI 783*x*R in a manner not specified in this document. Misuse of the NI 783*x*R can result in a hazard. You can compromise the safety protection built into the NI 783*x*R if the NI 783*x*R is damaged in any way. If the NI 783*x*R is damaged, return it to NI for repair.

Do *not* substitute parts or modify the NI 783*x*R except as described in this document. Use the NI 783*x*R only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the NI 783*x*R.

Do *not* operate the NI 783*x*R in an explosive atmosphere or where there might be flammable gases or fumes. If you must operate the NI 783*x*R in such an environment, it must be in a suitably rated enclosure.

If you need to clean the NI 783*x*R, use a soft, nonmetallic brush. Make sure that the NI 783*x*R is completely dry and free from contaminants before returning it to service.

Operate the NI 783*x*R only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- **Pollution Degree 1**—No pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- **Pollution Degree 2**—Only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation can be expected.
- **Pollution Degree 3**—Conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the NI 783*x*R is rated. Do *not* exceed the maximum ratings for the NI 783*x*R. Do not install wiring while the NI 783*x*R is live with electrical signals. Do not remove or add connector blocks when power is connected

to the system. Remove power from signal lines before connecting them to or disconnecting them from the NI 783*x*R.

Operate the NI 783*x*R at or below the *measurement category*[1] listed in the section *Maximum working voltage*, in Appendix A, *Specifications*. Measurement circuits are subjected to *working voltages*[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following list describes installation categories:

- **Measurement Category I**—Measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.
- **Measurement Category II**—Measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 V for U.S. or 230 V for Europe). Examples of Installation Category II are measurements performed on household appliances, portable tools, and similar products.
- **Measurement Category III**—Measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired equipment such as equipment in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus-bars, junction boxes, switches, socket-outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- **Measurement Category IV**—Measurements performed at the primary electrical supply installation (<1,000 V). Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

[1] Measurement categories, also referred to as *installation categories*, are defined in electrical safety standard IEC 61010-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers equipment. Suitably rated measuring circuits can be connected to the MAINS for measuring purposes.

2

Hardware Overview of the NI 783*x*R

This chapter presents an overview of the hardware functions and I/O connectors on the NI 783*x*R.

Figure 2-1 shows a block diagram for the NI 7830R. Figure 2-2 shows a block diagram for the NI 7831R/7833R.

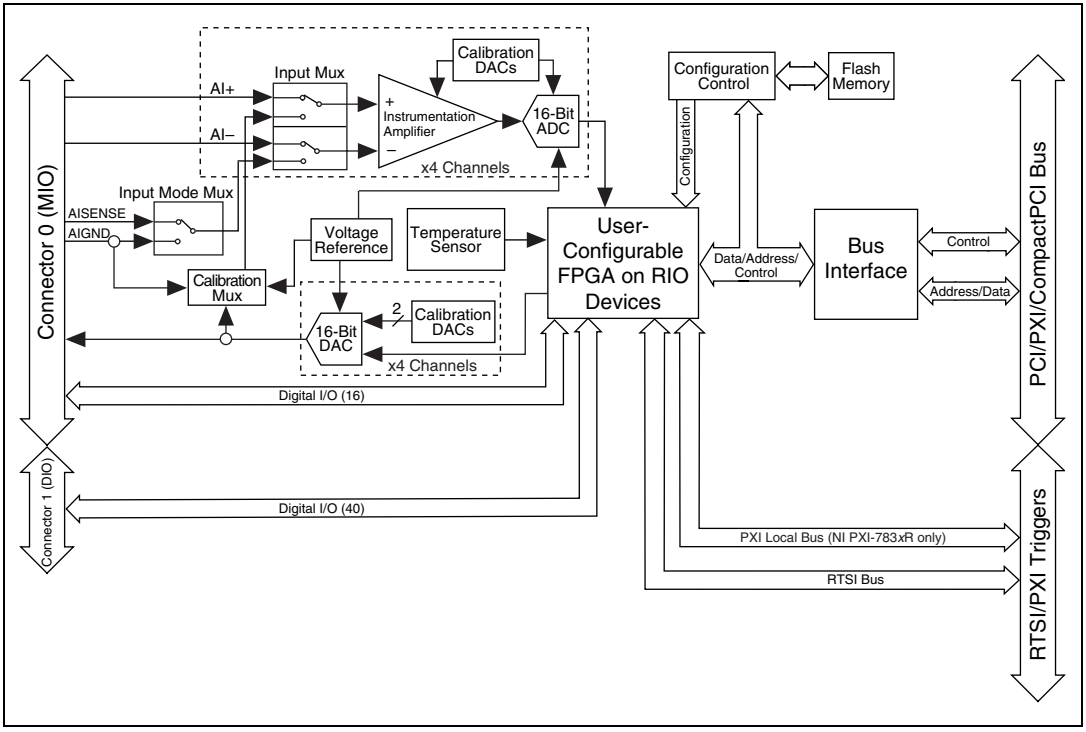


Figure 2-1. NI 7830R Block Diagram

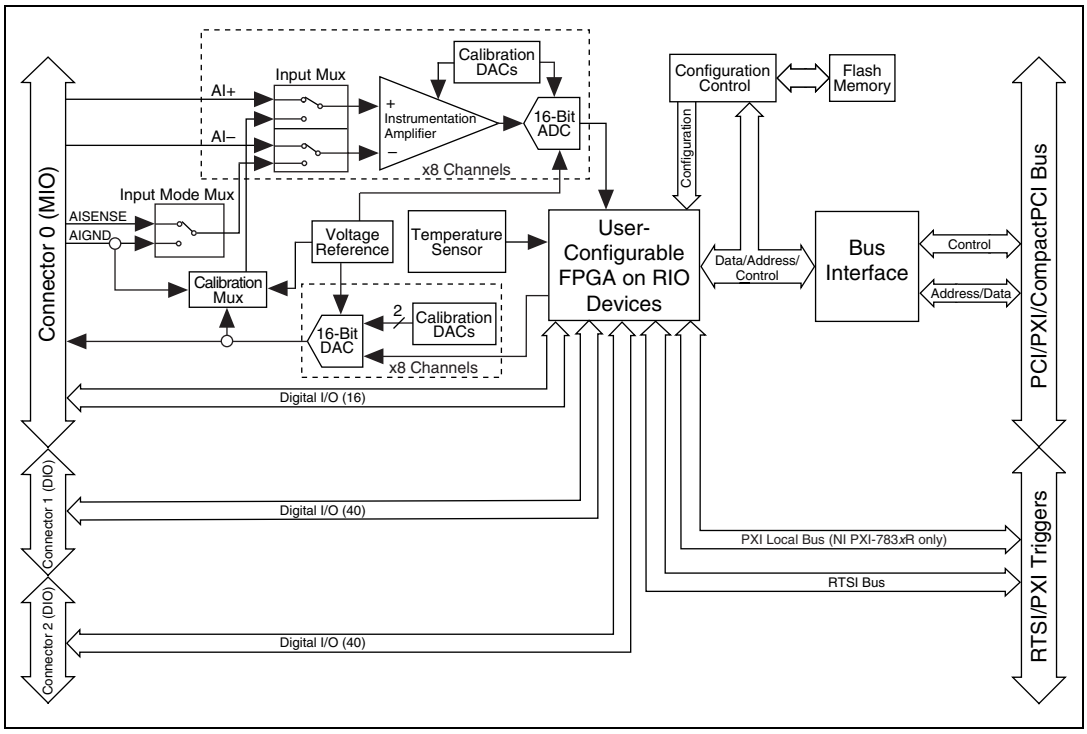


Figure 2-2. NI 7831R/7833R Block Diagram

NI 7830R Overview

The NI 7830R has four independent, 16-bit AI channels; four independent, 16-bit AO channels; and 56 bidirectional DIO lines that you can configure individually for input or output.

NI 7831R/7833R Overview

The NI 7831R and NI 7833R each have eight independent, 16 bit AI channels; eight independent, 16-bit AO channels; and 96 bidirectional DIO lines that you can configure individually for input or output.

Analog Input

You can sample NI 783*x*R AI channels simultaneously or at different rates. The input mode is software configurable, and the input range is fixed at

±10 V. The converters return data in two's complement format. Table 2-1 shows the ideal output code returned for a given AI voltage.

Table 2-1. Ideal Output Code and AI Voltage Mapping

Input Description	AI Voltage	Output Code (Hex) (Two's Complement)
Full-scale range –1 LSB	9.999695	7FFF
Full-scale range –2 LSB	9.999390	7FFE
Midscale	0.000000	0000
Negative full-scale range +1 LSB	–9.999695	8001
Negative full-scale range	–10.000000	8000
Any input voltage	$\frac{Output\ Code}{32{,}768} \times 10.0\ \text{V}$	—

Input Modes

The NI 783*x*R input mode is software configurable. The input channels support three input modes—differential (DIFF), referenced single ended (RSE), and nonreferenced single ended (NRSE). The selected input mode applies to all the input channels. Table 2-2 describes the three input modes.

Table 2-2. Available Input Modes for the NI 783*x*R

Input Mode	Description
DIFF	When the NI 783*x*R is configured in DIFF input mode, each channel uses two AI lines. The positive input pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input pin connects to the negative input of the instrumentation amplifier.
RSE	When the NI 783*x*R is configured in RSE input mode, each channel uses only its positive AI pin. This pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input of the instrumentation amplifier connects internally to the AI ground (AIGND).
NRSE	When the NI 783*x*R is configured in NRSE input mode, each channel uses only its positive AI pin. This pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input of the instrumentation amplifier on each AI channel connects internally to the AISENSE input pin.

Input Range

The NI 783*x*R AI range is fixed at ±10 V.

Connecting Analog Input Signals

The AI signals for the NI 783*x*R are AI<0..*n*>+, AI<0..*n*>–, AIGND, and AISENSE. For the NI 7830R, *n*=4. For the NI 7831R/7833R, *n*=8. The AI<0..*n*>+ and AI<0..*n*>– signals are connected to the eight AI channels of the NI 783*x*R. For all input modes, the AI<0..*n*>+ signals are connected to the positive input of the instrumentation amplifier on each channel. The signal connected to the negative input of the instrumentation amplifier depends on how you configure the input mode of the device.

In differential input mode, signals connected to AI<0..*n*>– are routed to the negative input of the instrumentation amplifier for each channel. In RSE input mode, the negative input of the instrumentation amplifier for each channel is internally connected to AIGND. In NRSE input mode, the AISENSE signal is connected internally to the negative input of the instrumentation amplifier for each channel. In DIFF and RSE input modes, AISENSE is not used.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the NI 783*x*R and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in Table B-2, *NI 783xR I/O Signal Summary*.

AIGND is a common AI signal that is routed directly to the ground tie point on the NI 783*x*R. You can use this signal for a general analog ground tie point to the NI 783*x*R if necessary.

Connection of AI signals to the NI 783*x*R depends on the input mode of the AI channels you are using and the type of input signal source. With different input modes, you can use the instrumentation amplifier in different ways. Figure 2-3 shows a diagram of the NI 783*x*R instrumentation amplifier.

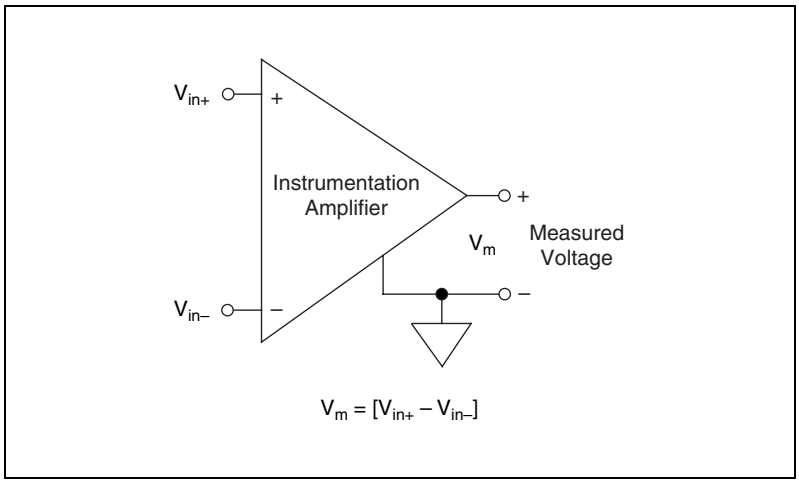


Figure 2-3. NI 783*x*R Instrumentation Amplifier

The instrumentation amplifier applies common-mode voltage rejection and presents high input impedance to the AI signals connected to the NI 783*x*R. Input multiplexers on the device route signals to the positive and negative inputs of the instrumentation amplifier. The instrumentation amplifier converts two input signals to a signal that is the difference between the two input signals. The amplifier output voltage is referenced to the device ground. The NI 783*x*R ADC measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the NI 783*x*R. If you have a floating source, reference the signal to ground by using RSE input mode or the DIFF input mode with bias resistors. Refer to the *Differential Connections for Nonreferenced or Floating Signal Sources* section of this chapter for more information about these input modes. If you have a grounded source, do not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input modes.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground referenced. The following sections describe these two signal types.

Floating Signal Sources

A floating signal source is not connected to the building ground system but instead has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must connect the ground reference of a floating signal to the NI 783*x*R AIGND through a bias resistor to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

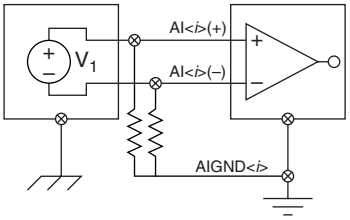
A ground-referenced signal source is connected to the building system ground, so it is already connected to a common ground point with respect to the NI 783*x*R, assuming that the computer is plugged into the same power system. Instruments or devices with nonisolated outputs that plug into the building power system are ground referenced signal sources.

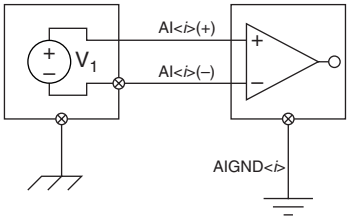
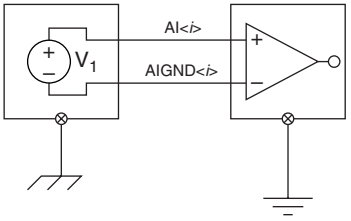
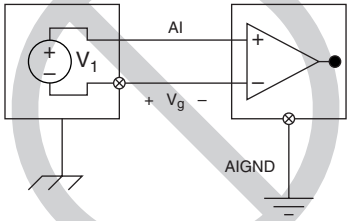
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV. This difference can be much higher if power distribution circuits are improperly connected. If a grounded signal source is improperly measured, this difference might appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

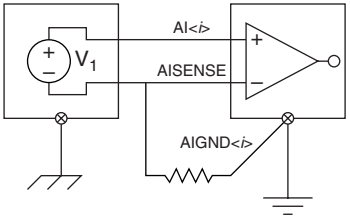
Input Modes

The following sections discuss single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Figure 2-4 summarizes the recommended input mode for both types of signal sources.

<table>
<tr><th rowspan="3">Input</th><th colspan="2">Signal Source Type</th></tr>
<tr><th>Floating Signal Source
(Not Connected to Building Ground)</th><th>Grounded Signal Source</th></tr>
<tr><td>Examples
• Ungrounded Thermocouples
• Signal Conditioning with Isolated Outputs
• Battery Devices</td><td>Examples
• Plug-in Instruments with Nonisolated Outputs</td></tr>
<tr><td>Differential (DIFF)</td><td> 

See text for information on bias resistors.</td><td> 
</td></tr>
<tr><td>Single-Ended — Ground Referenced (RSE)</td><td> 
</td><td>NOT RECOMMENDED
 

Ground-loop losses, V_g, are added to measured signal.</td></tr>
<tr><td>Single-Ended — Nonreferenced (NRSE)</td><td> 

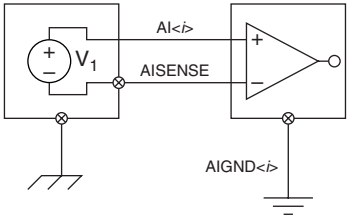
See text for information on bias resistors.</td><td> 
</td></tr>
</table>

Figure 2-4. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Mode)

In DIFF input mode, the NI 783*x*R measures the difference between the positive and negative inputs. DIFF input mode is ideal for measuring ground-referenced signals from other devices. When using DIFF input mode, the input signal connects to the positive input of the instrumentation amplifier and its reference signal, or return, connects to the negative input of the instrumentation amplifier.

Use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the NI 783*x*R are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce noise pickup and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the instrumentation amplifier.

Differential Connections for Ground-Referenced Signal Sources

Figure 2-5 shows how to connect a ground-referenced signal source to a channel on the NI 783*x*R configured in DIFF input mode.

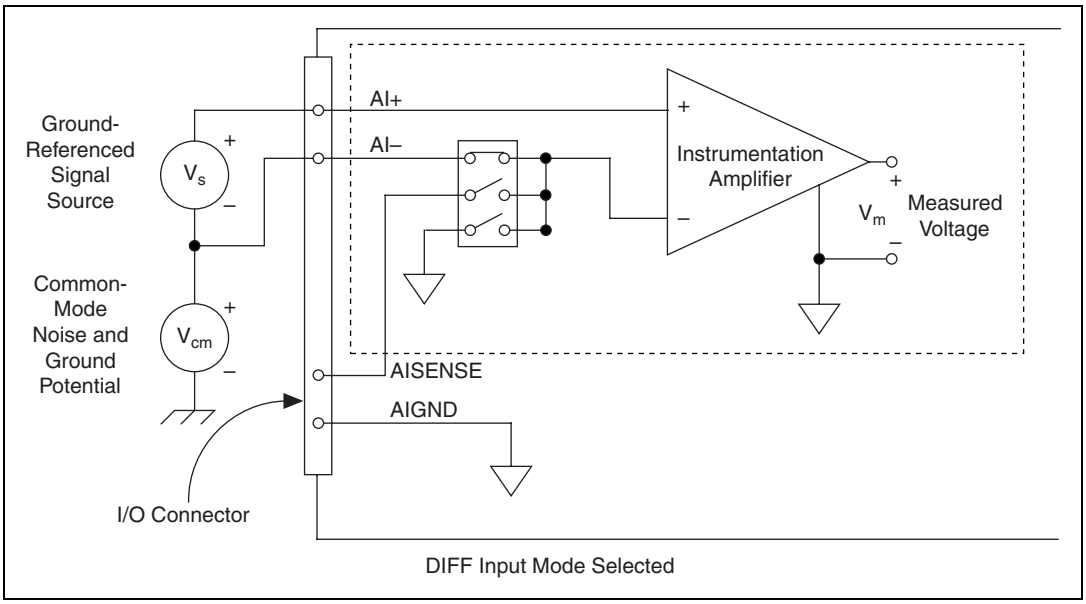


Figure 2-5. Differential Input Connections for Ground-Referenced Signals

With this connection type, the instrumentation amplifier rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the NI 783*x*R ground, shown as V_{cm} in Figure 2-5. In addition, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject common-mode signals when $V+_{in}$ and $V-_{in}$ (input signals) are both within their specified input ranges. Refer to Appendix A, *Specifications*, for more information about input ranges.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 2-6 shows how to connect a floating signal source to a channel on the NI 783*x*R configured in DIFF input mode.

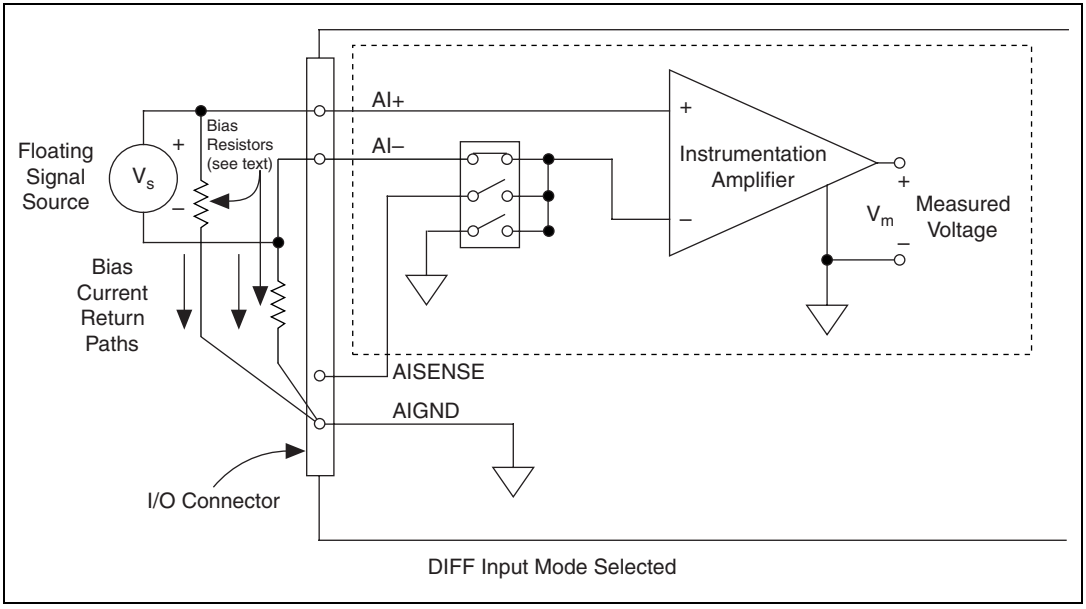


Figure 2-6. Differential Input Connections for Nonreferenced Signals

Figure 2-6 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source might not remain within the common-mode signal range of the instrumentation amplifier, causing erroneous readings. You must reference the source to AIGND by connecting the positive side of the signal to the positive input of the instrumentation amplifier and connecting the negative side of the signal to AIGND and to the negative input of the instrumentation amplifier without resistors. This connection works well for DC-coupled sources with low source impedance, less than 100 Ω.

For larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the instrumentation amplifier does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance. About the same amount of noise couples onto both connections, which yields better rejection of electrostatically coupled noise. Also, this input mode does not load down the source, other than the very high-input impedance of the instrumentation amplifier.

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 2-6. This fully balanced input mode offers slightly better noise rejection but has the disadvantage of loading down the source with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the instrumentation amplifier require a DC path to ground for the instrumentation amplifier to work. If the source is AC coupled (capacitively coupled), the instrumentation amplifier needs a resistor between the positive input and AIGND. If the source has low-impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current, typically 100 kΩ to 1 MΩ. In this case, connect the negative input directly to AIGND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs. Loading down the source causes some gain error.

Single-Ended Connection Considerations

When an NI 783*x*R AI signal is referenced to a ground that can be shared with other input signals, it forms a single-ended connection. The input signal connects to the positive input of the instrumentation amplifier and the ground connects to the negative input of the instrumentation amplifier.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high-level (>1 V).
- The leads connecting the signal to the NI 783*x*R are less than 3 m (10 ft).
- The input signal can share a common reference point with other signals.

Use DIFF input connections for greater signal integrity for any input signal that does not meet the preceding conditions.

You can configure the NI 783*x*R channels in software for RSE or NRSE input modes. Use the RSE input mode for floating signal sources. In this case, the NI 783*x*R provides the reference ground point for the external signal. Use the NRSE input mode for ground-referenced signal sources. In this case, the external signal supplies its own reference ground point and the NI 783*x*R should not supply one.

In single-ended input modes, electrostatic and magnetic noise couples into the signal connections more than in differential input modes. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Input Mode)

Figure 2-7 shows how to connect a floating signal source to a channel on the NI 783*x*R configured for RSE input mode.

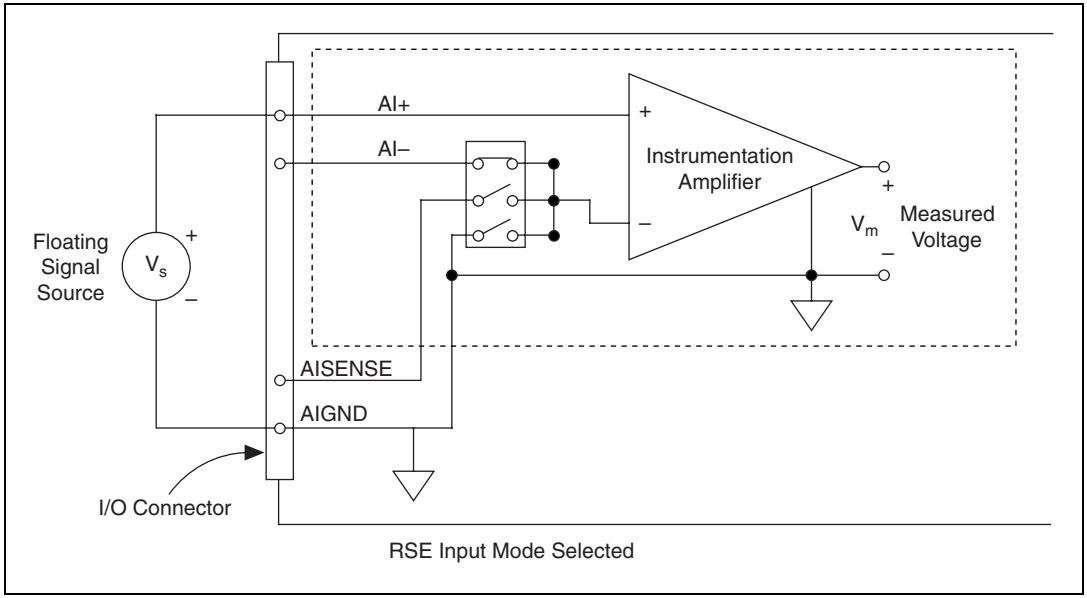


Figure 2-7. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Input Mode)

To measure a grounded signal source with a single-ended input mode, you must configure the NI 783*x*R in the NRSE input mode. Then connect the signal to the positive input of the NI 783*x*R instrumentation amplifier and connect the signal local ground reference to the negative input of the instrumentation amplifier. The ground point of the signal should be connected to AISENSE. Any potential difference between the NI 783*x*R ground and the signal ground appears as a common-mode signal at both the

positive and negative inputs of the instrumentation amplifier. The instrumentation amplifier rejects this difference. If the input circuitry of a NI 783*x*R is referenced to ground in RSE input mode, this difference in ground potentials appears as an error in the measured voltage.

Figure 2-8 shows how to connect a grounded signal source to a channel on the NI 783*x*R configured for NRSE input mode.

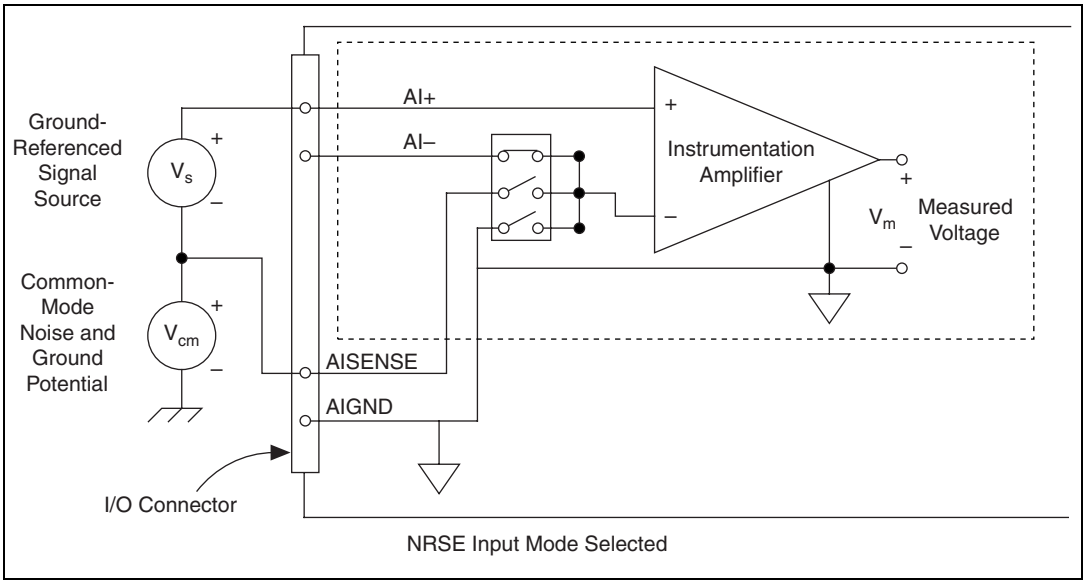


Figure 2-8. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figure 2-5 and Figure 2-8 show connections for signal sources that are already referenced to some ground point with respect to the NI 783*x*R. In these cases, the instrumentation amplifier can reject any voltage caused by ground potential differences between the signal source and the device. With differential input connections, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject common-mode signals when $V+_{in}$ and $V-_{in}$ (input signals) are both within their specified input ranges. Refer to Appendix A, *Specifications*, for more information about input ranges.

Analog Output

The bipolar output range of the NI 783*x*R AO channels is fixed at ±10 V. Some applications require that the AO channels power on to known voltage levels. To set the power-on levels, you can configure the NI 783*x*R to load and run a VI when the system powers on. The VI can set the AO channels to the desired voltage levels. The VI interprets data written to the DAC in two's complement format. Table 2-3 shows the ideal AO voltage generated for a given input code.

Table 2-3. Ideal Output Voltage and Input Code Mapping

Output Description	AO Voltage	Input Code (Hex) (Two's Complement)
Full-scale range –1 LSB	9.999695	7FFF
Full-scale range –2 LSB	9.999390	7FFE
Midscale	0.000000	0000
Negative full-scale range, +1 LSB	–9.999695	8001
Negative full-scale range	–10.000000	8000
Any output voltage	—	$\frac{AO\ Voltage}{10.0\ \text{V}} \times 32{,}768$

Note If your VI does not set the output value for an AO channel, then the AO channel voltage output will be undefined.

Connecting Analog Output Signals

The AO signals are AO <0..*n*> and AOGND.

AO <0..*n*> are the AO channels. AOGND is the ground reference signal for the AO channels.

Figure 2-9 shows how to make AO connections to the NI 783*x*R.

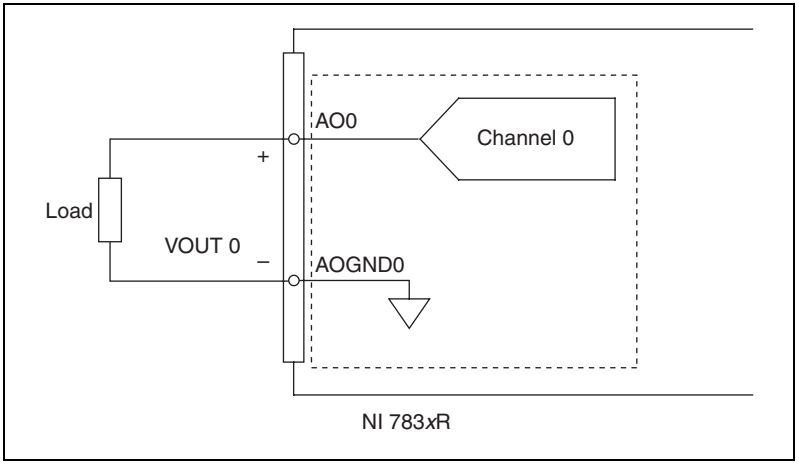


Figure 2-9. Analog Output Connections

Digital I/O

You can configure the NI 783*x*R DIO lines individually for either input or output. When the system powers on, the DIO lines are high impedance. To set another power-on state, you can configure the NI 783*x*R to load a VI when the system powers on. The VI can then set the DIO lines to any power-on state.

Connecting Digital I/O Signals

The DIO signals on the NI 783*x*R MIO connector are DGND and DIO<0..15>. The DIO signals on the NI 783*x*R DIO connector are DGND and DIO<0..39>. The DIO<0..*n*> signals make up the DIO port and DGND is the ground reference signal for the DIO port. The NI 7830R has one MIO and one DIO connector for a total of 56 DIO lines. The NI 7831R/7833R has one MIO and two DIO connectors for a total of 96 DIO lines.

Refer to Figure B-1, *NI 783xR Connector Locations*, and Figure B-2, *NI 783xR I/O Connector Pin Assignments*, for the connector locations and the I/O connector pin assignments on the NI 783*x*R.

The DIO lines on the NI 783*x*R are TTL-compatible. When configured as inputs, they can receive signals from 5 V TTL, 3.3 V LVTTL, 5 V CMOS, and 3.3 V LVCMOS devices. When configured as outputs, they can send signals to 5 V TTL, 3.3 V LVTTL, and 3.3 V LVCMOS devices. Because the digital outputs provide a nominal output swing of 0 to 3.3 V

(3.3 V TTL), the DIO lines cannot drive 5 V CMOS logic levels. To interface to 5 V CMOS devices, you must provide an external pull-up resistor to 5 V. This resistor pulls up the 3.3 V digital output from the NI 783*x*R to 5 V CMOS logic levels. Refer to Appendix A, *Specifications*, for detailed DIO specifications.

Caution Exceeding the maximum input voltage ratings, listed in Table B-2, *NI 783xR I/O Signal Summary*, can damage the NI 783*x*R and the computer. NI is *not* liable for any damage resulting from such signal connections.

Caution Do *not* short the DIO lines of the NI 783*x*R directly to power or to ground. Doing so can damage the NI 783*x*R by causing excessive current to flow through the DIO lines.

You can connect multiple NI 783*x*R digital output lines in parallel to provide higher current sourcing or sinking capability. If you connect multiple digital output lines in parallel, your application must drive all of these lines simultaneously to the same value. If you connect digital lines together and drive them to different values, excessive current can flow through the DIO lines and damage the NI 783*x*R. Refer to Appendix A, *Specifications*, for more information about DIO specifications. Figure 2-10 shows signal connections for three typical DIO applications.

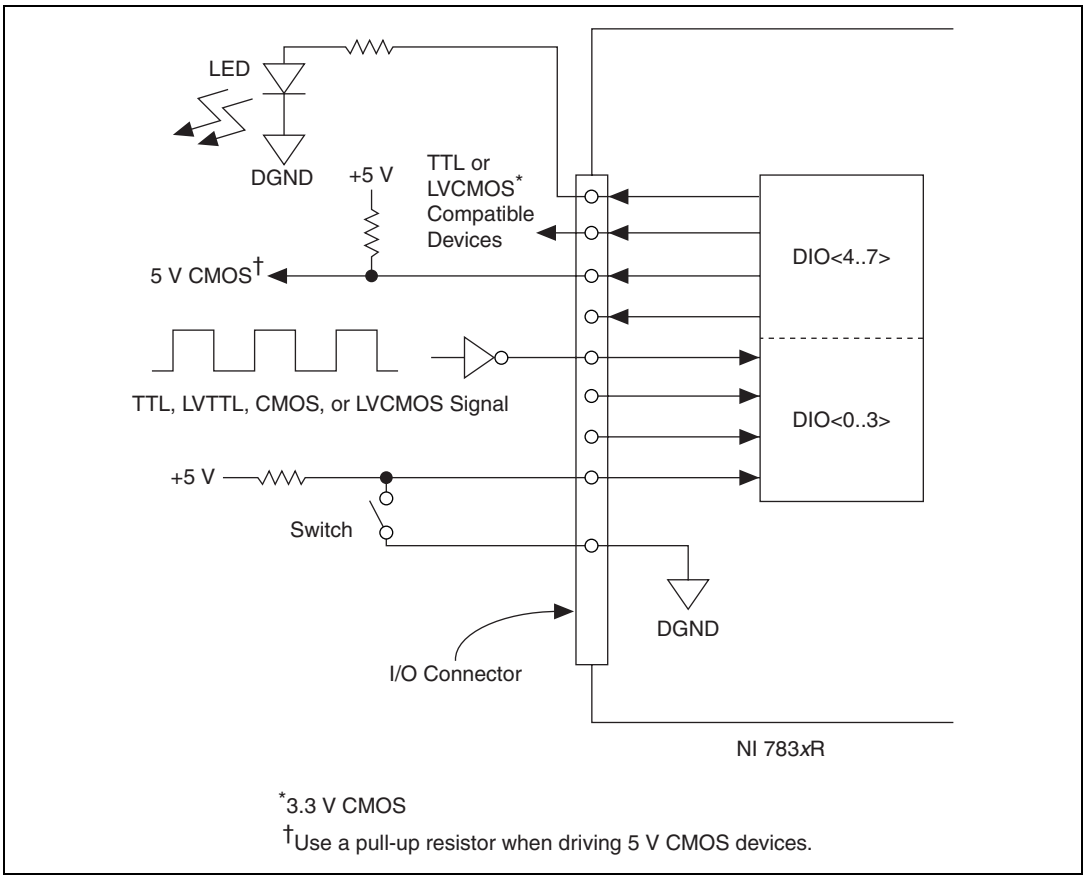


Figure 2-10. Example Digital I/O Connections

Figure 2-10 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL, LVTTL, CMOS, or LVCMOS signals and sensing external device states, such as the state of the switch shown in Figure 2-10. Digital output applications include sending TTL or LVCMOS signals and driving external devices, such as the LED shown in Figure 2-10.

The NI 783*x*R SH68-C68-S shielded cable contains 34 twisted pairs of conductors. To maximize the digital I/O available on the NI 783*x*R, some of the DIO lines are twisted with power or ground and some DIO lines are twisted with other DIO lines. To obtain maximum signal integrity, place edge-sensitive or high-frequency digital signals on the DIO lines that are paired with power or ground. Because the DIO lines that are twisted with other DIO lines can couple noise onto each other, use these lines for static

signals or non-edge-sensitive, low-frequency digital signals. Examples of high-frequency or edge-sensitive signals include clock, trigger, pulse-width modulation (PWM), encoder, and counter signals. Examples of static signals or non-edge-sensitive, low-frequency signals include LEDs, switches, and relays. Table 2-4 summarizes these guidelines.

Table 2-4. DIO Signal Guidelines for the NI 783*x*R

Digital Lines	SH68-C68-S Shielded Cable Signal Pairing	Recommended Types of Digital Signals
Connector 0, DIO<0..7>; Connector 1, DIO<0..27>; Connector 2, DIO<0..27>	DIO line paired with power or ground	All types—high-frequency or low-frequency signals, edge-sensitive or non-edge-sensitive signals
Connector 0, DIO<8..15>; Connector 1, DIO<28..39>; Connector 2, DIO<28..39>	DIO line paired with another DIO line	Static signals or non-edge-sensitive, low-frequency signals

RTSI Trigger Bus

The NI 783*x*R can send and receive triggers through the RTSI trigger bus. The RTSI bus provides eight shared triggers lines that connect to all the devices on the bus. In PXI, the trigger lines are shared between all the PXI slots in a bus segment. In PCI, the RTSI bus is implemented through a ribbon cable connected to the RTSI connector on each device that needs to access the RTSI bus.

You can use the RTSI trigger lines to synchronize the NI 783*x*R to any other device that supports RTSI triggers. On the NI PCI-783*x*R, the RTSI trigger lines are labeled RTSI/TRIG<0..6> and RTSI/OSC. On the NI PXI-783*x*R, the RTSI trigger lines are labeled PXI/TRIG<0..7>. In addition, the NI PXI-783*x*R can use the PXI star trigger line to send or receive triggers from a device plugged into Slot 2 of the PXI chassis. The PXI star trigger line on the NI PXI-783*x*R is PXI/STAR.

The NI 783*x*R can configure each RTSI trigger line either as an input or an output signal. Because each trigger line on the RTSI bus is connected in parallel to all the other RTSI devices on the bus, only one device should drive a particular RTSI trigger line at a time. For example, if one NI PXI-783*x*R is configured to send out a trigger pulse on PXI/TRIG0, the remaining devices on that PXI bus segment must have PXI/TRIG0 configured as an input.

Caution Do *not* drive the same RTSI trigger bus line with the NI 783*x*R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

For more information on using and configuring triggers, select **Help»VI, Function, & How-To Help** in LabVIEW to view the *LabVIEW Help*. Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

PXI Local Bus (for NI PXI-783*x*R only)

The NI PXI-783*x*R can communicate with other PXI devices using the PXI local bus. The PXI local bus is a daisy-chained bus that connects each PXI peripheral slot with its adjacent peripheral slot on either side. For example, the right local bus lines from a PXI peripheral slot connect to the left local bus lines of the adjacent slot on the right. Each local bus is 13 lines wide. All of these lines connect to the FPGA on the NI PXI-783*x*R. The PXI local bus right lines on the NI PXI-783*x*R are PXI/LBR<0..12>. The PXI local bus left lines on the NI PXI-783*x*R are PXI/LBLSTAR<0..12>.

The NI PXI-783*x*R can configure each PXI local bus line either as an input or an output signal. Only one device can drive the same physical local bus line at a time. For example, if the NI PXI-783*x*R is configured to drive a signal on PXI/LBR 0, the device in the slot immediately to the right must have its PXI/LBLSTAR 0 line configured as an input.

Caution Do *not* drive the same PXI local bus line with the NI PXI-783*x*R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

The NI PXI-783*x*R local bus lines are only compatible with 3.3 V signaling LVTTL and LVCMOS levels.

Caution Do *not* enable the local bus lines on an adjacent device if the device drives anything other than 0–3.3V LVTTL signal levels on the NI PXI-783*x*R. Enabling the lines in this way can damage the NI PXI-783*x*R. NI is *not* liable for any damage resulting from enabling such lines.

The left local bus lines from the left peripheral slot of a PXI backplane (Slot 2) are routed to the star trigger lines of up to 13 other peripheral slots in a two-segment PXI system. This configuration provides a dedicated,

delay-matched trigger signal between the first peripheral slot and the other peripheral slots for precise trigger timing signals. For example, an NI PXI-783*x*R in Slot 2 can send an independent trigger signal to each device plugged into Slots <3..15> using the PXI/LBLSTAR<0..12>. Each device receives its trigger signal on its own dedicated star trigger line.

Caution Do *not* configure the NI 783*x*R and another device to drive the same physical star trigger line simultaneously. Such signal driving can damage the NI 783*x*R and the other device. NI is *not* liable for any damage resulting from such signal driving.

Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

Switch Settings

Refer to Figure 2-11 for the location of switches on the NI PXI-783*x*R and Figure 2-12 for the location of switches on the NI PCI-783*x*R. For normal operation, SW1 is in the OFF position. To prevent a VI stored in Flash memory from loading to the FPGA at power up, move SW1 to the ON position, as shown in Figure 2-13. SW2 and SW3 are not connected.

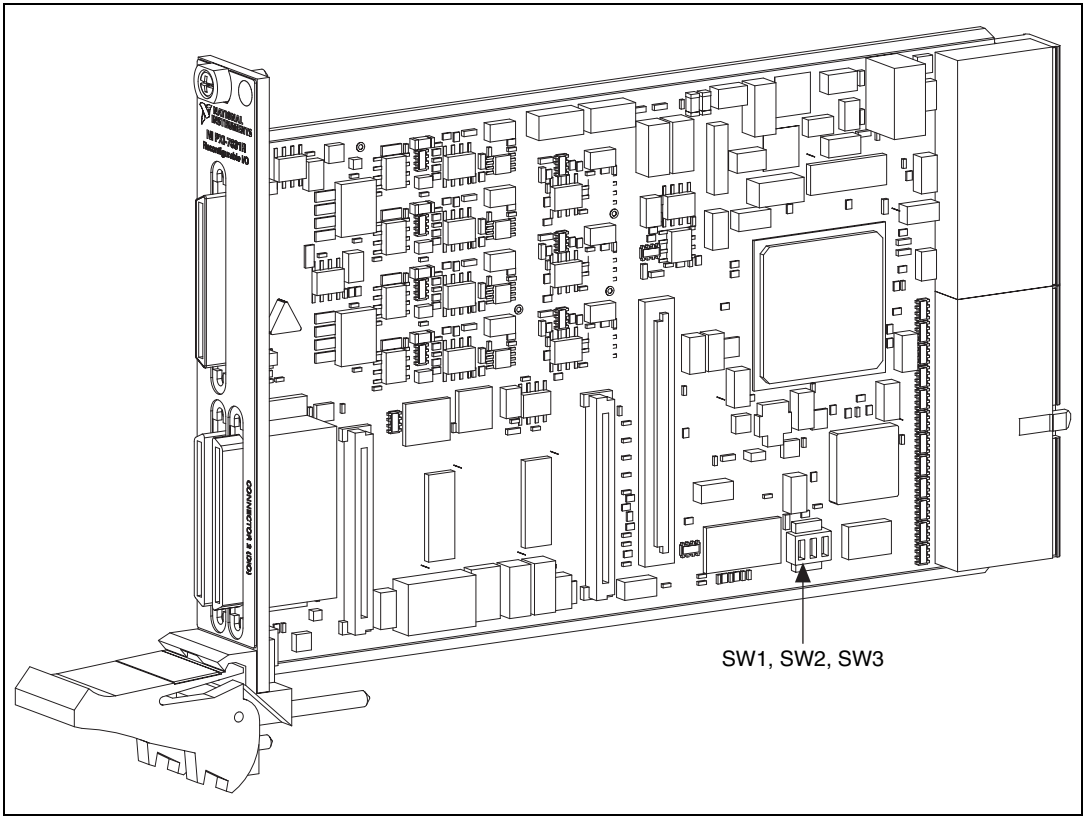


Figure 2-11. Switch Location on the NI PXI-783*x*R

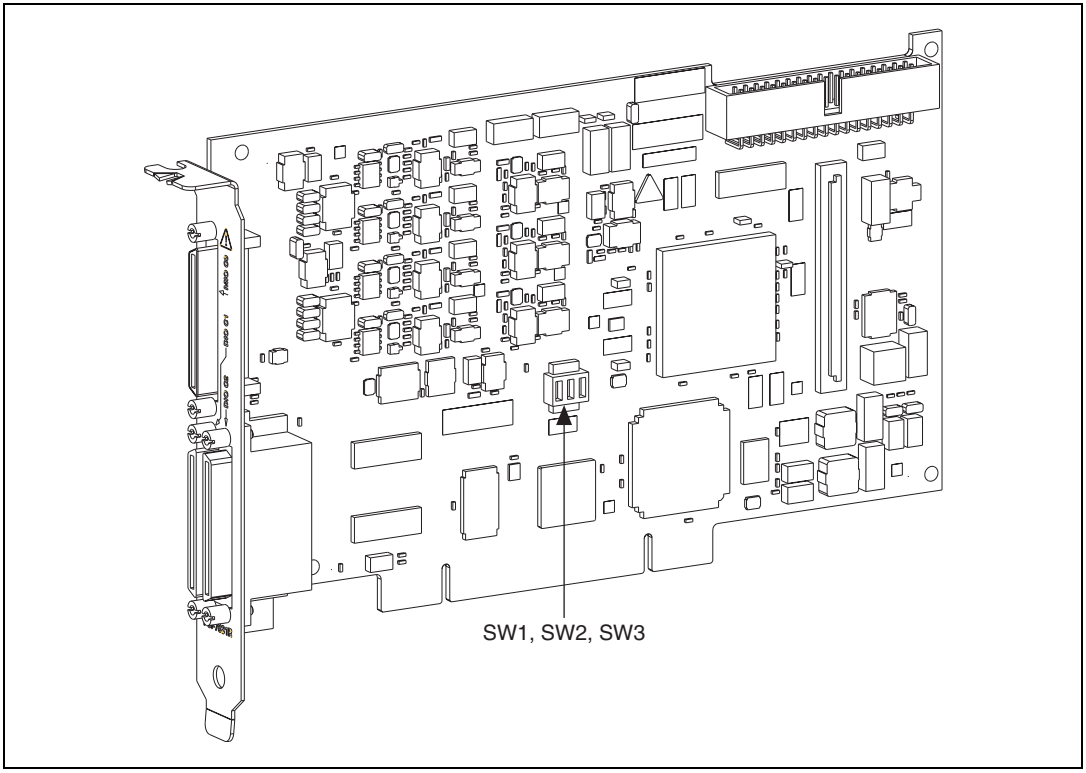


Figure 2-12. Switch Location on the NI PCI-783*x*R

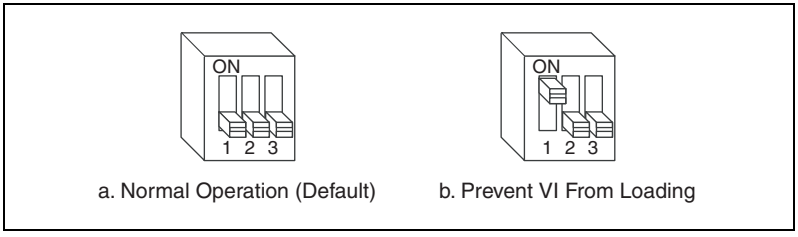


Figure 2-13. Switch Settings

Complete the following steps to prevent a VI stored in Flash memory from loading to the FPGA:

1. Power off and unplug the PXI/CompactPCI chassis or PCI computer.
2. Remove the NI 783*x*R from the PXI/CompactPCI chassis or PCI computer.
3. Move SW1 to the ON position, as shown in Figure 2-13b.

4. Reinsert the NI 783*x*R into the PXI/CompactPCI chassis or PCI computer. Refer to the *Installing the Hardware* section of the *Getting Started with the NI* 783*x*R document for installation instructions.
5. Plug in and power on the PXI/CompactPCI chassis or PCI computer.

After completing this procedure, a VI stored in Flash memory does not load to the FPGA at power-on. You can use software to configure the NI 783*x*R if necessary. To return to the defaults of loading from Flash memory, repeat the previous procedure but return SW1 to the OFF position in step 3. You can use this switch to enable/disable the ability to load from Flash memory. In addition to this switch, you must configure the NI 783*x*R with the software to autoload an FPGA VI.

Note When the NI 783*x*R is powered on with SW1 in the ON position, the analog circuitry does not return properly calibrated data. Move the switch to the ON position only while you are using software to reconfigure the NI 783*x*R for the desired power-up behavior. Afterward, return SW1 to the OFF position.

Power Connections

Two pins on each I/O connector supply 5 V from the computer power supply using a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. The +5V pins are referenced to DGND and can power external digital circuitry. The NI 783*x*R has the following power rating:

+4.50 to +5.25 VDC at 1 A (250 mA max per +5V pin, 1 A max total for all +5V lines on the device)

Caution Do *not* connect the +5V power pins directly to analog or digital ground or to any other voltage source on the NI 783*x*R or any other device under any circumstance. Doing so can damage the NI 783*x*R and the computer. NI is *not* liable for damage resulting from such a connection.

Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations mainly apply to AI signal routing to the device. They also apply to signal routing in general.

Take the following precautions to minimize noise pickup and maximize measurement accuracy:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the positive and negative inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PXI DAQ system is the video monitor. Keep the monitor and the analog signals as far apart as possible.

Use the following recommendations for all signal connections to the NI 783*x*R:

- Separate NI 783*x*R signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the NI 783*x*R signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

Refer to the NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone` for more information.

3

Calibration

Calibration is the process of determining and/or adjusting the accuracy of an instrument to minimize measurement and output voltage errors. On the NI 783*x*R, onboard calibration DACs (CalDACs) correct these errors. Because the analog circuitry handles calibration, the data read from the AI channels or written to the AO channels in the FPGA VI is already calibrated.

Three levels of calibration are available for the NI 783*x*R to ensure the accuracy of its analog circuitry. The first level, loading calibration constants, is the fastest, easiest, and least accurate. The intermediate level, internal calibration, is the preferred method of assuring accuracy in your application. The last level, external calibration, is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI 783*x*R is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The onboard nonvolatile Flash memory stores the calibration constants for the device. Calibration constants are the values that were written to the CalDACs to achieve calibration in the factory. The NI 783*x*R hardware reads these constants from the Flash memory and loads them into the CalDACs at power-on. This occurs before you load a VI into the FPGA.

Internal Calibration

With internal calibration, the NI 783*x*R can measure and correct almost all of its calibration-related errors without any external signal connections. NI provides software to perform an internal calibration. This internal calibration process, which generally takes less than two minutes, is the preferred method of assuring accuracy in your application. Internal calibration minimizes the effects of any offset and gain drifts, particularly those due to changes in temperature. During the internal calibration process, the AI and AO channels are compared to the NI 783*x*R onboard voltage reference. The offset and gain errors in the analog circuitry are calibrated out by adjusting the CalDACs to minimize these errors.

If you have NI-RIO installed, you can find the internal calibration utility at **Start»All Programs»National Instruments»NI-RIO»*device*»Calibrate 783*x*R Device**. *Device* is the NI PXI-783*x*R or NI PCI-783*x*R device.

Immediately after internal calibration, the only significant residual calibration error is gain error due to time and temperature drift of the onboard voltage reference. You can minimize gain errors by performing an external calibration. If you are primarily taking relative measurements, then you can ignore a small amount of gain error and self-calibration is sufficient.

The Flash memory on the NI 783*x*R stores the results of an internal calibration so the CalDACs automatically load with the newly calculated calibration constants the next time the NI 783*x*R is powered on.

External Calibration

An external calibration refers to calibrating your device with a known external reference rather than relying on the onboard reference. The NI 783*x*R has an onboard calibration reference to ensure the accuracy of self-calibration. The reference voltage is measured at the factory and stored in the Flash memory for subsequent internal calibrations. Externally calibrate the device annually or more often if you use it at extreme temperatures.

During the external calibration process, the onboard reference value is re-calculated. This compensates for any time or temperature drift-related errors in the onboard reference that might have occurred since the last calibration. You can save the results of the external calibration process to Flash memory so that the NI 783*x*R loads the new calibration constants the next time it is powered on. The device uses the newly measured onboard reference level for subsequent internal calibrations.

To externally calibrate your device, use an external reference several times more accurate than the device itself.

A

Specifications

This appendix lists the specifications of the NI 783*x*R. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels

- NI 7830R..... 4
- NI 7831R..... 8
- NI 7833R..... 8

Input modes..... DIFF, RSE, NRSE (software-selectable; selection applies to all channels)

Type of ADC..... Successive approximation

Resolution ..... 16 bits, 1 in 65,536

Conversion time ..... 4 µs

Maximum sampling rate ..... 200 kS/s (per channel)

Input impedance

- Powered on ..... 10 GΩ in parallel with 100 pF
- Powered off..... 4 kΩ min
- Overload..... 4 kΩ min

Input signal range..... ±10 V

Input bias current ..... ±2 nA

Input offset current..... ±1 nA

Input coupling ..... DC

Maximum working voltage
(signal + common mode).....Inputs should remain within ±12 V of ground

Overvoltage protection .....±42 V

Data transfers.....Interrupts, programmed I/O

Accuracy Information

Nominal Range (V)		Absolute Accuracy							Relative Accuracy	
		% of Reading			Noise + Quantization (µV)				Resolution (µV)	
Positive Full Scale	Negative Full Scale	24 Hours	1 Year	Offset (µV)	Single Point	Averaged	Temp Drift (%/°C)	Absolute Accuracy at Full Scale (±mV)	Single Point	Averaged
10.0	–10.0	0.0496	0.0507	2542	1779	165	0.0005	7.78	2170	217

Note: Accuracies are valid for measurements following an internal calibration. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature. Temp drift applies only if ambient is greater than ±10 °C of previous external calibration.

DC Transfer Characteristics

INL.....±3 LSB typ, ±6 LSB max

DNL .....–1.0 to +2.0 LSB max

No missing codes resolution.....16 bits typ, 15 bits min

CMRR, DC to 60 Hz .....86 dB

Dynamic Characteristics

Bandwidth

Small signal (–3 dB).....650 kHz

Large signal (1% THD).....55 kHz

System noise .....1.8 LSB_{rms} (including quantization)

Settling Time

Step Size	Accuracy		
	16 LSB	4 LSB	2 LSB
±20.0 V	7.5 µs	10.3 µs	40 µs
±2.0 V	2.7 µs	4.1 µs	5.1 µs
±0.2 V	1.7 µs	2.9 µs	3.6 µs

Crosstalk..... –80 dB, DC to 100 kHz

Analog Output

Output Characteristics

Output type..... Single-ended, voltage output

Number of channels

NI 7830R..... 4

NI 7831R..... 8

NI 7833R..... 8

Resolution ..... 16 bits, 1 in 65,536

Update time ..... 1.0 µs

Max update rate..... 1 MS/s

Type of DAC..... Enhanced R-2R

Data transfers ..... Interrupts, programmed I/O

Accuracy Information

Nominal Range (V)		Absolute Accuracy				Absolute Accuracy at Full Scale (mV)
		% of Reading				
Positive Full Scale	Negative Full Scale	24 Hours	1 Year	Offset (µV)	Temp Drift (%/°C)	
10.0	–10.0	0.0335	0.0351	2366	0.0005	5.88

Note: Accuracies are valid for analog output following an internal calibration. Analog output accuracies are listed for operation temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature. Temp Drift applies only if ambient is greater than ±10 °C of previous external calibration.

DC Transfer Characteristics

INL.....±0.5 LSB typ, ±4.0 LSB max

DNL.....±0.5 LSB typ, ±1 LSB max

Monotonicity .....16 bits, guaranteed

Voltage Output

Range .....±10 V

Output coupling .....DC

Output impedance.....1.25 Ω

Current drive.....±2.5 mA

Protection.....Short-circuit to ground

Power-on state .....User configurable

Dynamic Characteristics

Settling time

Step Size	Accuracy		
	16 LSB	4 LSB	2 LSB
±20.0 V	6.0 µs	6.2 µs	7.2 µs
±2.0 V	2.2 µs	2.9 µs	3.8 µs
±0.2 V	1.5 µs	2.6 µs	3.6 µs

Slew rate..... 10 V/µs

Noise ..... 150 μV_{rms}, DC to 1 MHz

Glitch energy
at midscale transition ..... ±200 mV for 3 µs

Digital I/O

Number of channels

NI 7830R..... 56
NI 7831R..... 96
NI 7833R..... 96

Compatibility ..... TTL

Digital logic levels

Level	Min	Max
Input low voltage (V_{IL})	0.0 V	0.8 V
Input high voltage (V_{IH})	2.0 V	5.5 V
Output low voltage (V_{OL}), where $I_{OUT} = -I_{max}$ (sink)	—	0.4 V
Output high voltage (V_{OH}), where $I_{OUT} = I_{max}$ (source)	2.4 V	—

Maximum output current

I_{max} (source)..... 5.0 mA
I_{max} (sink) ..... 5.0 mA

Input leakage current..... ±10 µA

Power-on state..... Programmable, by line

Data transfers ..... Interrupts, programmed I/O

Protection

Input..... –0.5 to 7.0 V
Output ..... Short-circuit (up to eight lines may be shorted at a time)

Reconfigurable FPGA

Number of logic slices
- NI 7830R 5,120
- NI 7831R 5,120
- NI 7833R 14,336

Equivalent number of logic cells
- NI 7830R 11,520
- NI 7831R 11,520
- NI 7833R 32,256

Available embedded RAM
- NI 7830R .....81,920 bytes
- NI 7831R .....81,920 bytes
- NI 7833R .....196,608 bytes

Timebase.....40, 80, 120, 160, or 200 MHz

Timebase reference sources
- NI PCI-783*x*R.....Onboard clock only
- NI PXI-783*x*R.....Onboard clock, phase-locked to PXI 10 MHz clock

Timebase accuracy
- Onboard clock .....±100 ppm, 250 ps jitter

Phase locked to PXI 10 MHz Clock (NI PXI-783*x*R only) .....Adds 350 ps jitter, 300 ps skew

Additional frequency dependent jitter
- 40 MHz.....None
- 80 MHz.....400 ps
- 120 MHz.....720 ps
- 160 MHz.....710 ps
- 200 MHz.....700 ps

Calibration

Recommended warm-up time.....15 minutes

Calibration interval.....1 year

Onboard calibration reference

DC level ..... 5.000 V (±3.5 mV) (actual value stored in Flash memory)

Temperature coefficient ..... ±5 ppm/°C max

Long-term stability ..... $\pm 20 \text{ ppm}/\sqrt{1{,}000 \text{ h}}$

Note Refer to **Calibration Certificates** at `ni.com/calibration` to generate a calibration certificate for the NI 783*x*R.

Bus Interface

PXI (NI PXI-783*x*R only) ..... Master, slave

PCI (NI PCI-783*x*R only) ..... Master, slave

Power Requirement

+5 VDC (±5%)

NI 7830R..... 330 mA (typ), 355 mA (max)[1]

NI 7831R..... 330 mA (typ), 355 mA (max)[1]

NI 7833R..... 364 mA (typ), 586 mA (max)[1]

+3.3 VDC (±5%)

NI 7830R..... 462 mA (typ), 660 mA (max)[2]

NI 7831R..... 462 mA (typ), 660 mA (max)[2]

NI 7833R..... 727 mA (typ), 1,148 mA (max)[2]

To calculate the total current sourced by the digital outputs use the following equation:

$$\sum_{i=1}^{j} \text{current sourced on channel } i$$

Where *j* is the number of digital outputs being used to source current.

Power available at I/O connectors ..... 4.50 to 5.25 VDC at 1 A total, 250 mA per I/O connector pin

[1] Does not include current drawn form the +5 V line on the I/O connectors.

[2] Does not include current sourced by the digital outputs.

Physical

Dimensions (not including connectors)

NI PXI-783*x*R.....16 cm by 10 cm (6.3 in. by 3.9 in.)

NI PCI-783*x*R.....17 cm by 11 cm (6.7 in. by 4.3 in.)

I/O connectors.....Three 68-pin female high-density VHDCI type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth .....±12 V, Measurement Category I

Channel-to-channel.....±24 V, Measurement Category I

Caution Do *not* use the NI 783*x*R for connection to signals in Measurement Categories II, III, or IV.

Environmental

The NI 783*x*R is intended for indoor use only.

Operating Environment

NI 7830R, NI 7831R

40 MHz or 80 MHz timebase .....0 °C to 55 °C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2

NI 7833R

40 MHz timebase.....0 °C to 55 °C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2

80 MHz timebase.....0 °C to 55 °C except the following: 0 °C to 45 °C when installed in an NI PXI-1000/B or NI PXI-101X; tested in accordance with IEC-60068-2-1 and IEC-60068-2-2

Relative humidity range ..... 10% to 90%, noncondensing, tested in accordance with IEC-60068-2-56

Altitude..... 2,000 m at 25 °C ambient temperature

Storage Environment

Ambient temperature range..... –20 °C to 70 °C tested in accordance with IEC-60068-2-1 and IEC-60068-2-2

Relative humidity range ..... 5% to 95%, noncondensing, tested in accordance with IEC-60068-2-56

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Shock and Vibration (for NI PXI-783*x*R Only)

Operational Shock..... 30 g peak, half-sine, 11 ms pulse Tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.

Random Vibration

Operating ..... 5 Hz to 500 Hz, 0.3 g_{rms}

Nonoperating ..... 5 Hz to 500 Hz, 2.4 g_{rms} Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Safety

The NI 783*x*R is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No. 61010-1

Note Refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column for UL and other safety certifications.

Electromagnetic Compatibility

Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz
Immunity	EN 61326:1997 + A2: 2001, Table 1
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) compliant

Note For full EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety)	73/23/EEC
Electromagnetic Compatibility Directive (EMC)	89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. Visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column to obtain the DoC for this product.

B

Connecting I/O Signals

This appendix describes how to make input and output signal connections to the NI 783*x*R I/O connectors.

Figure B-1 shows the I/O connector locations for the NI PXI-7831R/7833R and the NI PCI-7831R/7833R. The NI PXI-7830R and NI PCI-7830R do not have Connector 2 (DIO).

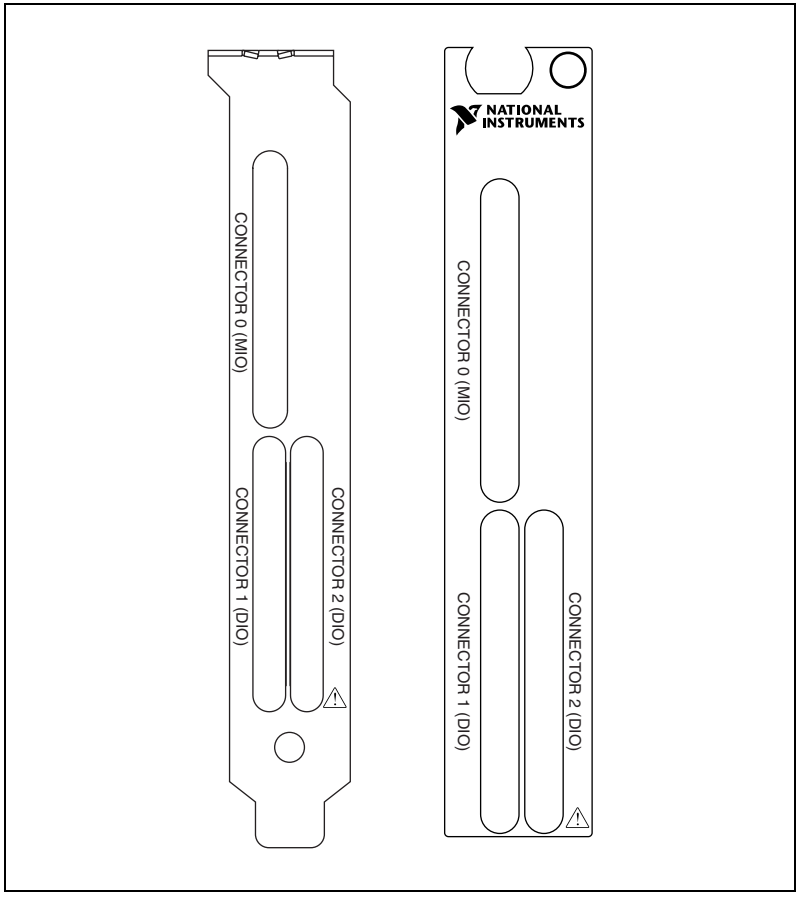


Figure B-1. NI 783*x*R Connector Locations

Figure B-2 shows the I/O connector pin assignments for the I/O connectors on the NI 783*x*R. The DIO connector pin assignment applies to connector 1 on the NI 7830R and connectors <1..2> on the NI 7831R/7833R.

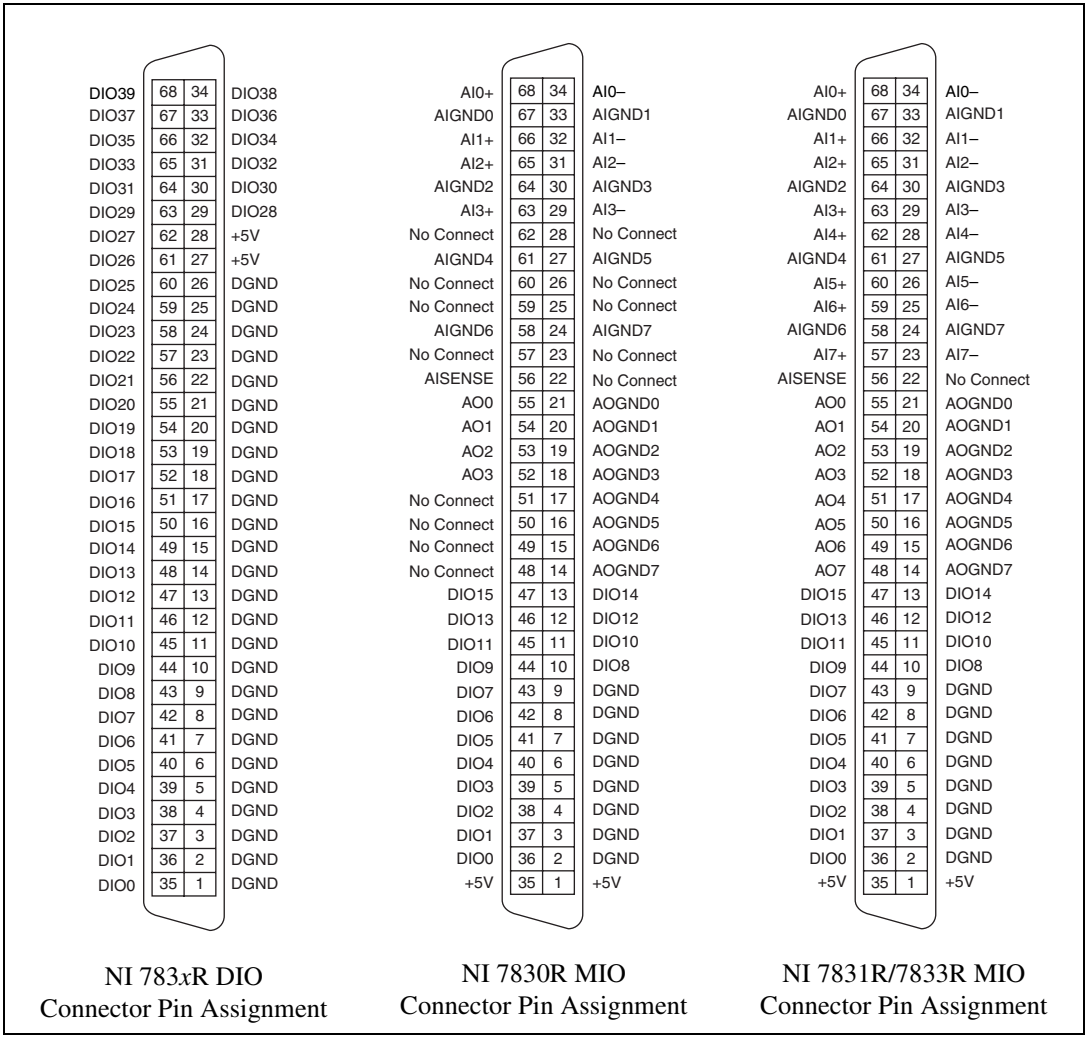

DIO39 68 34 DIO38
DIO37 67 33 DIO36
DIO35 66 32 DIO34
DIO33 65 31 DIO32
DIO31 64 30 DIO30
DIO29 63 29 DIO28
DIO27 62 28 +5V
DIO26 61 27 +5V
DIO25 60 26 DGND
DIO24 59 25 DGND
DIO23 58 24 DGND
DIO22 57 23 DGND
DIO21 56 22 DGND
DIO20 55 21 DGND
DIO19 54 20 DGND
DIO18 53 19 DGND
DIO17 52 18 DGND
DIO16 51 17 DGND
DIO15 50 16 DGND
DIO14 49 15 DGND
DIO13 48 14 DGND
DIO12 47 13 DGND
DIO11 46 12 DGND
DIO10 45 11 DGND
DIO9 44 10 DGND
DIO8 43 9 DGND
DIO7 42 8 DGND
DIO6 41 7 DGND
DIO5 40 6 DGND
DIO4 39 5 DGND
DIO3 38 4 DGND
DIO2 37 3 DGND
DIO1 36 2 DGND
DIO0 35 1 DGND
AI0+ 68 34 AI0–
AIGND0 67 33 AIGND1
AI1+ 66 32 AI1–
AI2+ 65 31 AI2–
AIGND2 64 30 AIGND3
AI3+ 63 29 AI3–
No Connect 62 28 No Connect
AIGND4 61 27 AIGND5
No Connect 60 26 No Connect
No Connect 59 25 No Connect
AIGND6 58 24 AIGND7
No Connect 57 23 No Connect
AISENSE 56 22 No Connect
AO0 55 21 AOGND0
AO1 54 20 AOGND1
AO2 53 19 AOGND2
AO3 52 18 AOGND3
No Connect 51 17 AOGND4
No Connect 50 16 AOGND5
No Connect 49 15 AOGND6
No Connect 48 14 AOGND7
DIO15 47 13 DIO14
DIO13 46 12 DIO12
DIO11 45 11 DIO10
DIO9 44 10 DIO8
DIO7 43 9 DGND
DIO6 42 8 DGND
DIO5 41 7 DGND
DIO4 40 6 DGND
DIO3 39 5 DGND
DIO2 38 4 DGND
DIO1 37 3 DGND
DIO0 36 2 DGND
+5V 35 1 +5V
AI0+ 68 34 AI0–
AIGND0 67 33 AIGND1
AI1+ 66 32 AI1–
AI2+ 65 31 AI2–
AIGND2 64 30 AIGND3
AI3+ 63 29 AI3–
AI4+ 62 28 AI4–
AIGND4 61 27 AIGND5
AI5+ 60 26 AI5–
AI6+ 59 25 AI6–
AIGND6 58 24 AIGND7
AI7+ 57 23 AI7–
AISENSE 56 22 No Connect
AO0 55 21 AOGND0
AO1 54 20 AOGND1
AO2 53 19 AOGND2
AO3 52 18 AOGND3
AO4 51 17 AOGND4
AO5 50 16 AOGND5
AO6 49 15 AOGND6
AO7 48 14 AOGND7
DIO15 47 13 DIO14
DIO13 46 12 DIO12
DIO11 45 11 DIO10
DIO9 44 10 DIO8
DIO7 43 9 DGND
DIO6 42 8 DGND
DIO5 41 7 DGND
DIO4 40 6 DGND
DIO3 39 5 DGND
DIO2 38 4 DGND
DIO1 37 3 DGND
DIO0 36 2 DGND
+5V 35 1 +5V
NI 783xR DIO Connector Pin Assignment
NI 7830R MIO Connector Pin Assignment
NI 7831R/7833R MIO Connector Pin Assignment

Figure B-2. NI 783*x*R I/O Connector Pin Assignments

To access the signals on the I/O connectors, you must connect a cable from the I/O connector to a signal accessory. Plug the small VHDCI connector end of the cable into the appropriate I/O connector and connect the other end of the cable to the appropriate signal accessory.

Table B-1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
+5V	DGND	Output	+5 VDC Source—These pins supply 5 V from the computer power supply using a self-resetting 1 A fuse. No more than 250 mA should be pulled from a single pin.
AI<0..7>+	AIGND	Input	Positive input for Analog Input channels 0 through 7.
AI<0..7>–	AIGND	Input	Negative input for Analog Input channels 0 through 7.
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected to each other on the NI 783*x*R.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for AI <0..7> when the device is configured for NRSE mode.
AO<0..7>	AOGND	Output	Analog Output channels 0 through 7. Each channel can source or sink up to 2.5 mA.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected to each other on the NI 783*x*R.
DGND	—	—	Digital Ground—These pins supply the reference for the digital signals at the I/O connector and the 5 V supply. All three ground references—AIGND, AOGND, and DGND—are connected to each other on the NI 783*x*R.
DIO<0..15> Connector 0 DIO<0..39> Connector <1..2>	DGND	Input or Output	Digital I/O signals.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 783*x*R can damage the NI 783*x*R and the computer. Maximum input ratings for each signal are in the *Protection* column of Table B-2. NI is *not* liable for any damage resulting from such signal connections

Table B-2. NI 783*x*R I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time	Bias
+5V	DO	—	—	—	—	—	—
AI<0..7>+	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AI<0..7>–	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AIGND	AO	—	—	—	—	—	—
AISENSE	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AO<0..7>	AO	1.25 Ω	Short circuit to ground	2.5 at 10	2.5 at –10	10 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
DIO<0..15> Connector 0 DIO<0..39> Connector <1..2>	DIO	—	–0.5 to +7.0	5.0 at 2.4	5.0 at 0.4	12 ns	—
AI = Analog Input AO = Analog Output DIO = Digital Input/Output DO = Digital Output							

Connecting to CompactRIO Extension I/O Chassis

You can use the CompactRIO R Series Expansion chassis and CompactRIO I/O modules with the NI 783*x*R. Refer to the *CompactRIO R Series Expansion System Installation Instructions* for information about connecting the chassis to the NI 783*x*R.

Connecting to 5B and SSR Signal Conditioning

NI provides cables that allow you to connect signals from the NI 783*x*R directly to 5B backplanes for analog signal conditioning and SSR backplanes for digital signal conditioning.

The NSC68-262650 cable connects the signals on the NI 783*x*R MIO connector directly to 5B and SSR backplanes. This cable has a 68-pin male VHDCI connector on one end that plugs into the NI 783*x*R MIO connector. The other end of this cable provides two 26-pin female headers plus one 50-pin female header.

One of the 26-pin headers contains all the NI 783*x*R analog input signals. You can plug this connector directly into a 5B backplane for analog input signal conditioning. The NI 783*x*R AI<0..*n*> correspond to the 5B backplane channels <0..*n*> in sequential order. Configure the AI channels to use the NRSE input mode when using 5B signal conditioning.

The other 26-pin header contains all the NI 783*x*R analog output signals. You can plug this connector directly into a 5B backplane for AO signal conditioning. The NI 783*x*R AO<0..*n*> correspond to the 5B backplane channels <0..*n*> in sequential order.

The 50-pin header contains the 16 DIO lines available on the NI 783*x*R MIO connector. You can plug this header directly into an SSR backplane for digital signal conditioning. DIO lines <0..15> correspond to the 5B backplane Slots <0..15> in sequential order.

The 5B connector pinouts are compatible with eight-channel 5B08 backplanes and 16-channel 5B01 backplanes. The NI 7830R can accept analog input from the first four channels of a 16-channel backplane. The NI 7831R/7833R can accept analog input from the first eight channels of a 16-channel backplane. The SSR connector pinout is compatible with eight-, 16-, 24-, and 32-channel SSR backplanes. You can connect to an SSR backplane containing a number of channels unequal to the 16 DIO lines available on the 50-pin header. In this case, you have access to only the channels that exist on both the SSR backplane and the NSC68-262650 cable 50-pin header.

Figure B-3 shows the connector pinouts when using the NSC68-262650 cable.

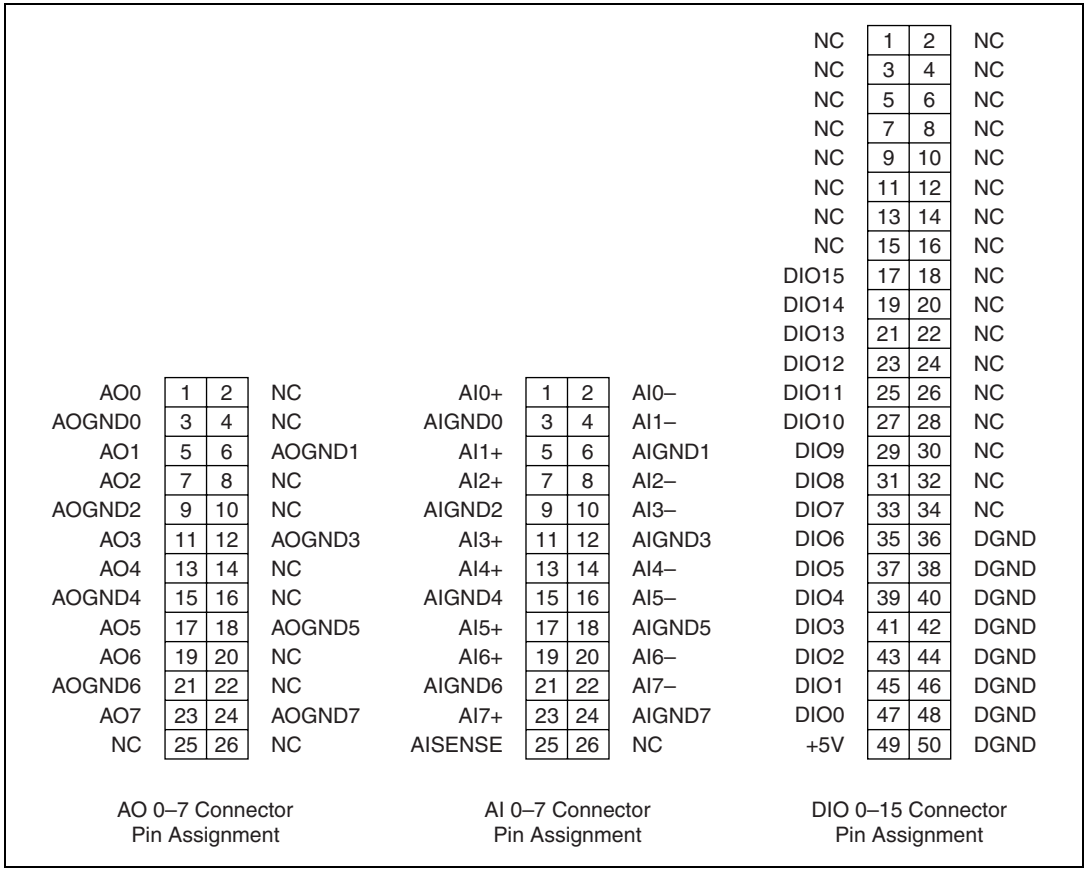

AO0 1 2 NC
AOGND0 3 4 NC
AO1 5 6 AOGND1
AO2 7 8 NC
AOGND2 9 10 NC
AO3 11 12 AOGND3
AO4 13 14 NC
AOGND4 15 16 NC
AO5 17 18 AOGND5
AO6 19 20 NC
AOGND6 21 22 NC
AO7 23 24 AOGND7
NC 25 26 NC
AO 0–7 Connector Pin Assignment
AI0+ 1 2 AI0–
AIGND0 3 4 AI1–
AI1+ 5 6 AIGND1
AI2+ 7 8 AI2–
AIGND2 9 10 AI3–
AI3+ 11 12 AIGND3
AI4+ 13 14 AI4–
AIGND4 15 16 AI5–
AI5+ 17 18 AIGND5
AI6+ 19 20 AI6–
AIGND6 21 22 AI7–
AI7+ 23 24 AIGND7
AISENSE 25 26 NC
AI 0–7 Connector Pin Assignment
NC 1 2 NC
NC 3 4 NC
NC 5 6 NC
NC 7 8 NC
NC 9 10 NC
NC 11 12 NC
NC 13 14 NC
NC 15 16 NC
DIO15 17 18 NC
DIO14 19 20 NC
DIO13 21 22 NC
DIO12 23 24 NC
DIO11 25 26 NC
DIO10 27 28 NC
DIO9 29 30 NC
DIO8 31 32 NC
DIO7 33 34 NC
DIO6 35 36 DGND
DIO5 37 38 DGND
DIO4 39 40 DGND
DIO3 41 42 DGND
DIO2 43 44 DGND
DIO1 45 46 DGND
DIO0 47 48 DGND
+5V 49 50 DGND
DIO 0–15 Connector Pin Assignment

Figure B-3. Connector Pinouts when Using NSC68-262650 Cable

The NSC68-5050 cable connects the signals on the NI 783*x*R DIO connectors directly to SSR backplanes for digital signal conditioning. This cable has a 68-pin male VHDCI connector on one end that plugs into the NI 783*x*R DIO connectors. The other end of this cable provides two 50-pin female headers.

You can plug each of these 50-pin headers directly into an 8-, 16-, 24-, or 32-channel SSR backplane for digital signal conditioning. One of the 50-pin headers contains DIO<0..23> from the NI 783*x*R DIO connector. These lines correspond to Slots <0..23> on an SSR backplane in sequential order. The other 50-pin header contains DIO<24..39> from the NI 783*x*R DIO connector. These lines correspond to Slots <0..15> on an SSR backplane in sequential order. You can connect to an SSR backplane containing a number of channels unequal to the number of lines on the

NSC68-5050 cable header. In this case, you have access only to the channels that exist on both the SSR backplane and the NSC68-5050 cable header you are using.

Figure B-4 shows the connector pinouts when using the NSC68-5050 cable.

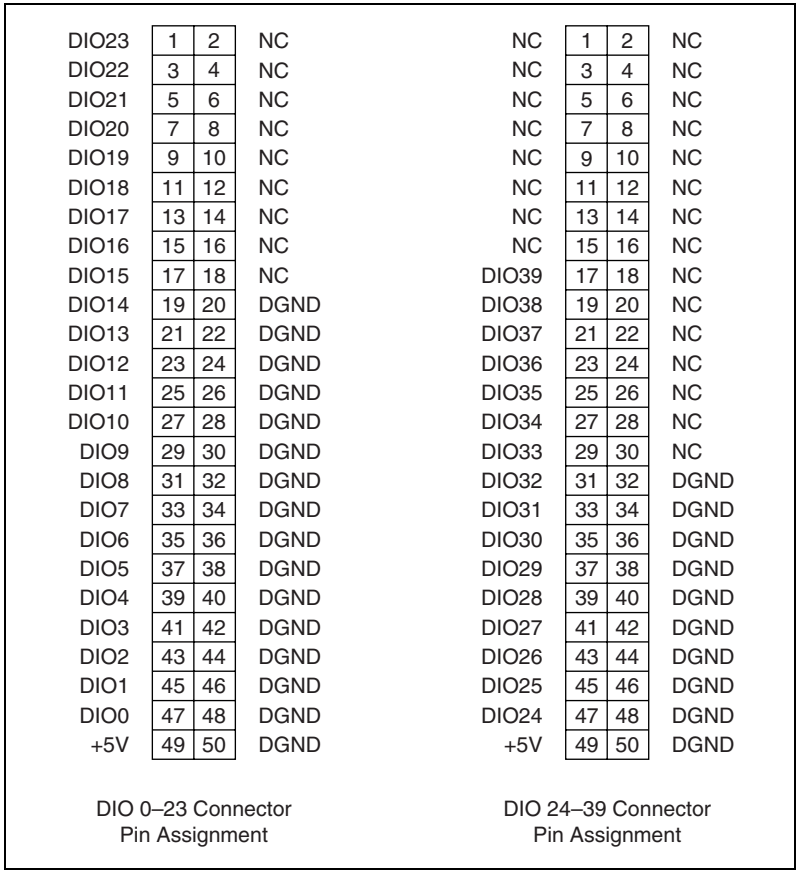

DIO23 1 2 NC
DIO22 3 4 NC
DIO21 5 6 NC
DIO20 7 8 NC
DIO19 9 10 NC
DIO18 11 12 NC
DIO17 13 14 NC
DIO16 15 16 NC
DIO15 17 18 NC
DIO14 19 20 DGND
DIO13 21 22 DGND
DIO12 23 24 DGND
DIO11 25 26 DGND
DIO10 27 28 DGND
DIO9 29 30 DGND
DIO8 31 32 DGND
DIO7 33 34 DGND
DIO6 35 36 DGND
DIO5 37 38 DGND
DIO4 39 40 DGND
DIO3 41 42 DGND
DIO2 43 44 DGND
DIO1 45 46 DGND
DIO0 47 48 DGND
+5V 49 50 DGND
DIO 0–23 Connector Pin Assignment
NC 1 2 NC
NC 3 4 NC
NC 5 6 NC
NC 7 8 NC
NC 9 10 NC
NC 11 12 NC
NC 13 14 NC
NC 15 16 NC
DIO39 17 18 NC
DIO38 19 20 NC
DIO37 21 22 NC
DIO36 23 24 NC
DIO35 25 26 NC
DIO34 27 28 NC
DIO33 29 30 NC
DIO32 31 32 DGND
DIO31 33 34 DGND
DIO30 35 36 DGND
DIO29 37 38 DGND
DIO28 39 40 DGND
DIO27 41 42 DGND
DIO26 43 44 DGND
DIO25 45 46 DGND
DIO24 47 48 DGND
+5V 49 50 DGND
DIO 24–39 Connector Pin Assignment

Figure B-4. Connector Pinouts when Using the NSC68-5050 Cable

C

Using the SCB-68 Shielded Connector Block

This appendix describes how to connect input and output signals to the NI 783*x*R with the SCB-68 shielded connector block.

The SCB-68 has 68 screw terminals for I/O signal connections. To use the SCB-68 with the NI 783*x*R, you must configure the SCB-68 as a general-purpose connector block. Refer to Figure C-1 for the general-purpose switch configuration.

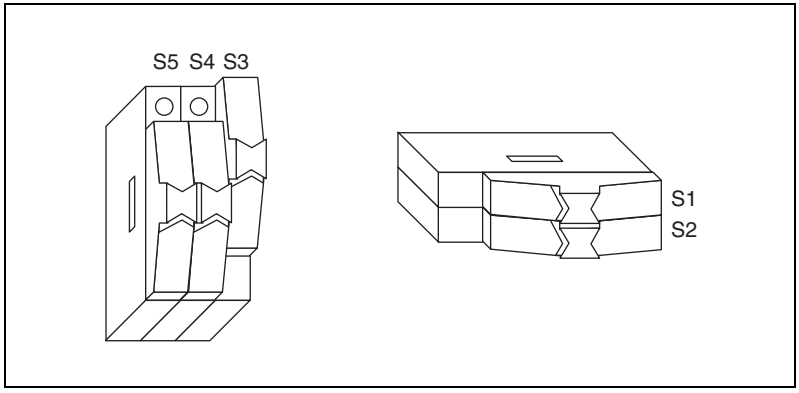


Figure C-1. General-Purpose Switch Configuration for the SCB-68 Terminal Block

After configuring the SCB-68 switches, you can connect the I/O signals to the SCB-68 screw terminals. Refer to Appendix B, *Connecting I/O Signals*, for the connector pin assignments for the NI 783*x*R. After connecting I/O signals to the SCB-68 screw terminals, you can connect the SCB-68 to the NI 783*x*R with the SH68-C68-S shielded cable.

D

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}

Numbers/Symbols

°	Degrees.
>	Greater than.
≥	Greater than or equal to.
<	Less than.
≤	Less than or equal to.
–	Negative of, or minus.
Ω	Ohms.
/	Per.
%	Percent.
±	Plus or minus.
+	Positive of, or plus.

$\sqrt{\ }$	Square root of.
+5V	+5 VDC source signal.

A

A	Amperes.
A/D	Analog-to-digital.
AC	Alternating current.
ADC	Analog-to-digital converter—An electronic device, often an integrated circuit, that converts an analog voltage to a digital number.
AI	Analog input.
AI<*i*>	Analog input channel signal.
AIGND	Analog input ground signal.
AISENSE	Analog input sense signal.
AO	Analog output.
AO<*i*>	Analog output channel signal.
AOGND	Analog output ground signal.
ASIC	Application-Specific Integrated Circuit—A proprietary semiconductor component designed and manufactured to perform a set of specific functions.

B

bipolar	A signal range that includes both positive and negative values (for example, –5 to +5 V).

C

C	Celsius.
CalDAC	Calibration DAC.
CH	Channel—Pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
cm	Centimeter.
CMOS	Complementary metal-oxide semiconductor.
CMRR	Common-mode rejection ratio—A measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB).
common-mode voltage	Any voltage present at the instrumentation amplifier inputs with respect to amplifier ground.
CompactPCI	Refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG).

D

D/A	Digital-to-analog.
DAC	Digital-to-analog converter—An electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.
DAQ	Data acquisition—A system that uses the computer to collect, receive, and generate electrical signals.
dB	Decibel—The unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts.
DC	Direct current.
DGND	Digital ground signal.
DIFF	Differential mode.

DIO	Digital input/output.
DIO<*i*>	Digital input/output channel signal.
DMA	Direct memory access—A method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	Differential nonlinearity—A measure in LSB of the worst-case deviation of code widths from their ideal value of 1 LSB.
DO	Digital output.

E

EEPROM	Electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed.

F

FPGA	Field-Programmable Gate Array.
FPGA VI	A configuration that is downloaded to the FPGA and that determines the functionality of the hardware.

G

glitch	An unwanted signal excursion of short duration that is usually unavoidable.

H

h	Hour.
HIL	Hardware-in-the-loop.
Hz	Hertz.

I

I/O	Input/output—The transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces.
INL	Relative accuracy.

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench. LabVIEW is a graphical programming language that uses icons instead of lines of text to create programs.
LSB	Least significant bit.

M

m	Meter.
max	Maximum.
MIMO	Multiple input, multiple output.
min	Minimum.
MIO	Multifunction I/O.
monotonicity	A characteristic of a DAC in which the analog output always increases as the values of the digital code input to it increase.
mux	Multiplexer—A switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.

N

noise	An undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	Nonreferenced single-ended mode—All measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

OUT	Output pin—A counter output pin where the counter can generate various TTL pulse waveforms.

P

PCI	Peripheral Component Interconnect—A high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations. PCI offers a theoretical maximum transfer rate of 132 MB/s.
port	(1) A communications connection on a computer or a remote controller. (2) A digital port, consisting of four or eight lines of digital input and/or output.
ppm	Parts per million.
pu	Pull-up.
PWM	Pulse-width modulation.
PXI	PCI eXtensions for Instrumentation—An open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

R

RAM	Random-access memory—The generic term for the read/write memory that is used in computers. RAM allows bits and bytes to be written to it as well as read from. Various types of RAM are DRAM, EDO RAM, SRAM, and VRAM.
resolution	The smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
RIO	Reconfigurable I/O.
rms	Root mean square.
RSE	Referenced single-ended mode—All measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.
RTSI	Real-time system integration bus—The timing and triggering bus that connects multiple devices directly. This allows for hardware synchronization across devices.

S

s	Seconds.
S	Samples.
S/s	Samples per second—Used to express the rate at which a DAQ board samples an analog signal.
signal conditioning	The manipulation of signals to prepare them for digitizing.
slew rate	The voltage rate of change as a function of time. The maximum slew rate of an amplifier is often a key specification to its performance. Slew rate limitations are first seen as distortion at higher signal frequencies.

T

THD	Total harmonic distortion—The ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage.
thermocouple	A temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TTL	Transistor-transistor logic.
two's complement	Given a number x expressed in base 2 with n digits to the left of the radix point, the (base 2) number $2n - x$.

V

V	Volts.
VDC	Volts direct current.
VHDCI	Very high density cabled interconnect.
VI	Virtual instrument—Program in LabVIEW that models the appearance and function of a physical instrument.
V_{IH}	Volts, input high.
V_{IL}	Volts, input low.
V_{OH}	Volts, output high.
V_{OL}	Volts, output low.
V_{rms}	Volts, root mean square.

W

waveform	Multiple voltage readings taken at a specific sampling rate.